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A 0.5V TRANSCONDUCTANCE ENHANCED RFC (TRFC) OTA

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Abstract:

This paper talks about a Recycling Folded Cascode Operational Transconductance Amplifier (RFC OTA) that uses low voltage and low power with a high transconductance. In order to improve the transconductance, a new input stage with a DC current source and a floating voltage source (FVS) is shown. There is a lot of DC biassing current split up because an FVS is used to connect the inner and outer pairs of input stages. This leads to a rise in the gain factor of the mirrors that recycle the current. This leads to a rise in the transconductance of the mirrors. An FVS can be changed to change the range of transconductance that can be achieved. This is what makes the structure unique.

Keywords: transconductance, DC biasing, floating voltage source etc

Transconductance Enhancement Method:

Previous chapters talked about how the value of parameter K is limited on the upside. This means that RFC transconductance can only be twice the FC transconductance, but it can't be more than that. Split the current in a way that will raise the value of parameter K, it is said. RFC OTA input stage transistor aspect ratios are set as (1 – x): (x), where the value of the input stage transistor ranges from zero to one. This is shown in figure 4.1. When the recycling current mirror transistors are used, the current path is changed to (2 x): (1 x): (1 x). This keeps the DC current the same. AFVS, VB, are used to make sure that the input stage gets a lot of power. FVS can be used to change the transconductance of the TRFC OTA, so that it can be changed.

An FVS splits a DC biasing current $2I_b$ disproportionately between an inner and outer differential pair comprising the transistors M1a-M2a and M1b-M2b respectively. The adoption of the FVS discriminates an effective overdrive voltage of transistors M1a-M2a and M1b-M2b as V_{gs} and $V_g - V_B$ respectively. The DC biasing current is split disproportionately during the input stage for an identical input voltage. As depicted in Fig.4.2, the FVS is implemented using the PMOS transistor MB. By varying the overdrive voltage VC of transistor MB, disproportionate current splitting in the input stage is achieved.

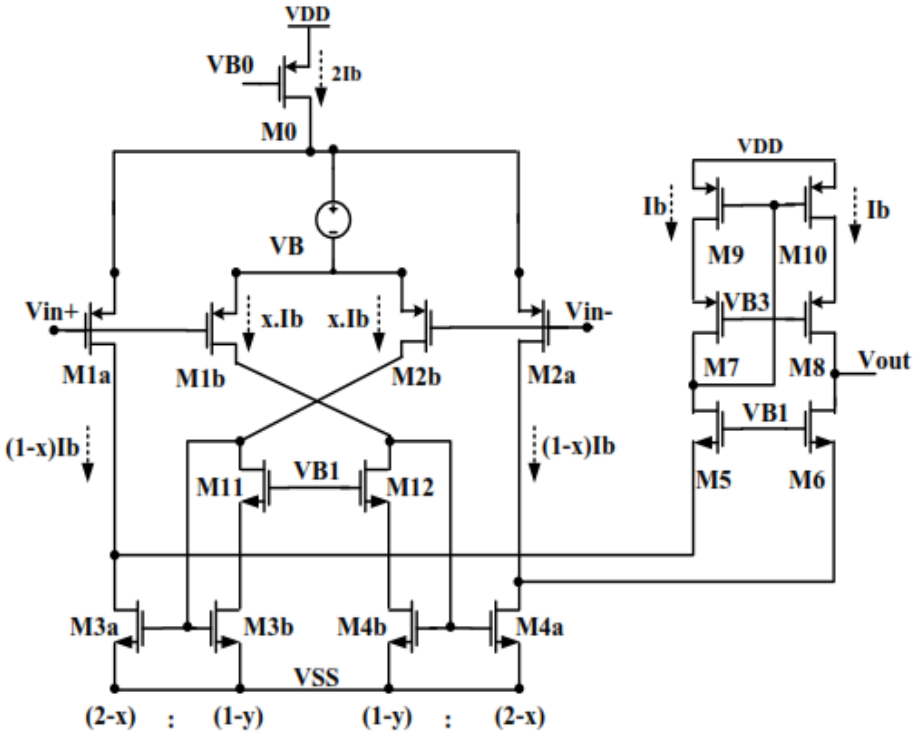

Figure 4.1. Transconductance Enhanced RFC (TRFC) OTA

An efficacious transconductance of the TRFC OTA is given in (4.1) as,

$$G_{mTRFC} = \left[(1-x) + \frac{(2-x)}{(1-y)}\right] g_m \qquad (4.1)$$

Where, g_m is the transconductance of the unsplit differential pair, which is the value of gm. G_{mTRFC} can be changed from g m1a to infinity by changing the value of the parameter x by the FVS, which is how you change the value of the parameter x. A smaller value of parameter x can be used to get a much bigger transconductance. Because a non-dominant pole is added to the OTA due to the recycling current mirror, the phase margin of the OTA will be pushed down into the low frequency range. Because a very high transconductance value makes the OTA unstable.

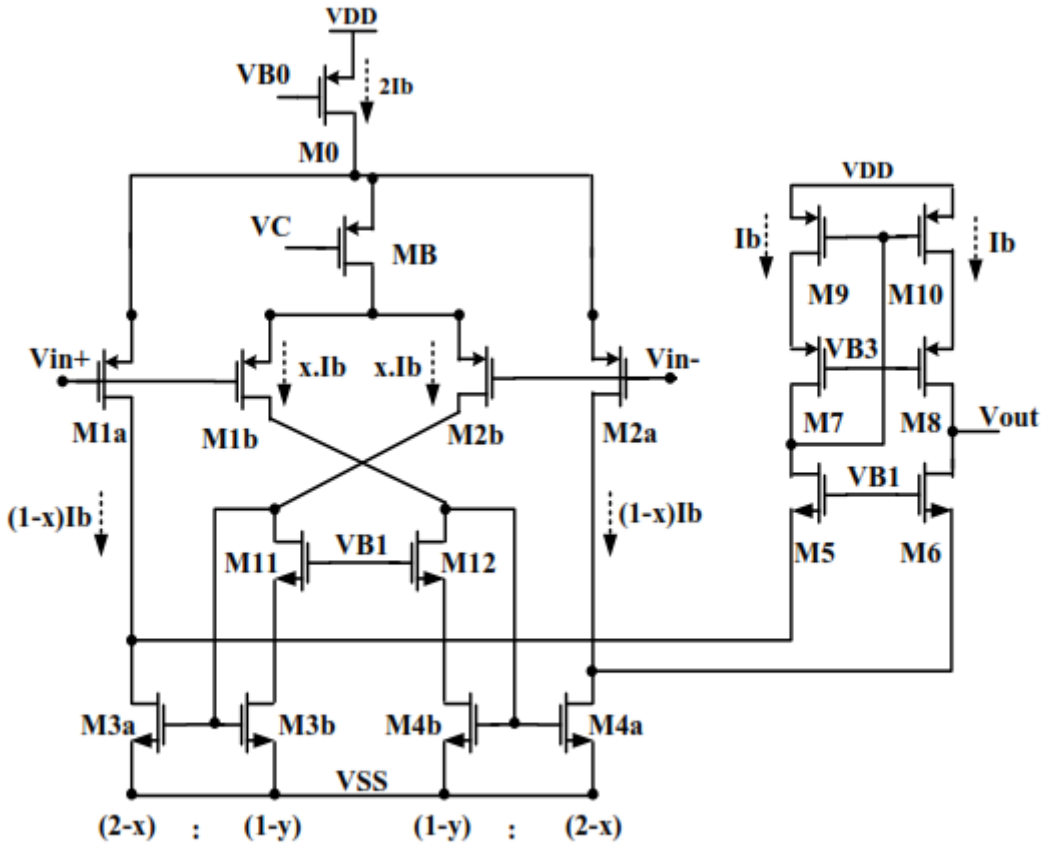

Figure 4.2. TRFC OTA with VB implementation

Next, we talk about how the better transconductance affects many of the OTA's performance parameters.

The performance of the TRFC OTA:

(a) Small Gain in Frequency as well as GBW:

The gain of the TRFC OTA can be represented as,

$$A_v = G_{mTRFC} R_{out}$$

$$A_v = \left[(1-x) + \frac{(2-x)}{(1-y)}\right] g_m [g_{m6} r_{06} (r_{o2a} || r_{o4a}) || g_{m8} r_{08} r_{o10}] \quad (4.2)$$

The gain enhancement is a reflection of the increase in transconductance. Additionally, the cascode load arrangement improves the output resistance. The combined effect of the increased transconductance and output impedance significantly increases the total gain of the TRF OTA. The TRFC OTA's GBW is shown in (4.3) as,

$$GBW_{TRFC} = \frac{G_{mTRFC}}{2\pi C_L} \quad (4.3)$$

Appropriate selection of parameter x significantly increases the gain and GBW of the TRFC OTA with a tolerable phase margin.

(b) Rate of slew:

The TRFC OTA's transient response to a big input signal is examined in this section:

When the input signal is large enough, the input stage transistors M1a and M1b enter the off state. This effectively disables transistors M4a and M4b, relocating transistors M2a and M6 into the deep triode and cut off regions, respectively. The whole tail current 2Ib runs through the transistor M2b and is available to charge the capacitor CL via the following transistors: M3b, M3a, and M5. As shown in Equation (4.4), the TRFC OTA's slew rate (SR) is as follows:

$$SR_{TRFC} = 2\,\frac{(2-x)I_b}{(1-y)C_L} \tag{4.4}$$

In comparison to the standard FC and RFC structures, the TRFC OTA gives a substantially larger SR for an adequate value of parameter x and a constant tail current. However, in comparison to a strong inversion region MOS transistor, an OTA has a lower SR due to the relatively low current conduction.

(c) Stability:

The stability of an amplifier is expressed in terms of its phase margin, which is primarily determined by the amount of zeros and poles introduced in its transfer function. Fig. 4.3 depicts the pole zero map for the proposed TRFC OTA. As illustrated in Figure 4.3, the proposed TRFC OTA, like the RFC OTA, consists of a single dominant pole P1, two non-dominant poles P2, P3, and a zero Z1. The pole P1 is connected to an output node defined by the OTA's output resistance Rout and an externally attached load capacitor CL. This is denoted by,

$$P_1 = \frac{1}{R_{out}C_L} \tag{4.5}$$

Equation (4.6) expresses the additional pole-zero pair set by a recycling current mirror as:

$$P_2 = \frac{(1-y)g_{m3,4b}}{[(2-x)+(1-y)]C_{gs3,4}} \tag{4.6}$$

$$Z_1 = \left[(1-x)+\frac{(2-x)}{(1-y)}\right]P_2 \tag{4.7}$$

As with the FC OTA, the second non-dominant pole, P3, occurs at the folding nodes and is denoted by,

$$P_3 = \frac{g_{m5,6}}{C_{gs5,6}+C_{db(2a,4a)}} \tag{4.8}$$

To maintain OTA stability, P2> 3 GBW must be met, which restricts the TRFC OTA's transconductance enhancement. As a result, the value of parameter x must be carefully set in order to balance the phase margin degradation and transconductance enhancement.

(d) Noise:

Noise is an important component to consider when designing analogue circuits with low voltage and low power. The thermal noise current can be expressed as, in the case of a MOS transistor.

$$\overline{i_o^2} = 4kT\gamma g_m$$

where k, T, and gm denote the Boltzmann constant, absolute temperature, and the transistor's transconductance, respectively. The value of parameter changes from 1/2 to 2/3, and the inversion region transitions from weak to strong. In the instance of the proposed TRFC OTA, the output thermal noise is denoted by the following equation (4.9):

$$\overline{V_{oTRFC}^2} = 2 * 4kT\gamma \left[\begin{matrix}(1-x)g_{m1a} + (2-x)g_{m3a} + g_{m9} + \\ \left(\frac{1-x}{1-y}\right)^2 [x.g_{m2b} + (1-y).g_{m3b}]\end{matrix}\right] * R_{out}^2 \tag{4.9}$$

Thus, for the TRFC, the thermal noise at the input is denoted as:

$$\overline{V_{iTRFC}^2} = \frac{\overline{V_{oTRFC}^2}}{A_v^2} \quad (4.10)$$

Since, $g_{mb1} = g_{mb2}$, $g_{mb1} = (1-x)g_{ma1}$ and $g_{m3a} = \left(\frac{2-x}{1-y}\right) g_{m3b}$

The input referred noise can be stated as follows for the proposed TRFC OTA:

$$\overline{V_{iTRFC}^2} = \frac{8KT\gamma}{\left((1-x)+\frac{2-x}{1-y}\right)^2 g_{m1}} \left\{\left[1+\frac{(2-x)^2}{x}\right](1-x) + 2(2-x)\frac{g_{m3a}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right\} \quad (4.11)$$

In comparison to the FC and RFC OTAs, the TRFC OTA has a somewhat greater input referred noise due to the recycling current mirror's enhanced gain factor, which amplifies the noise current of transistors M1b and M2b. However, the increased transconductance and low-threshold MOS transistor contribute greatly to its noise reduction.

(e) Power efficiency:

The power efficiency (PE) of an amplifier is defined as the ratio of its transconductance to the current consumed. The planned TRFC OTA's PE is as follows:

$$PE = \frac{G_{mTRFC}}{2I_b} \quad (4.12)$$

Due to the increased transconductance, the TRFC OTA achieves a higher power efficiency than the FC and RFC OTA for the same tail current value.

Implementation and Results:

The FC, RFC, and TRFC OTAs are designed and simulated using a 0.18um TSMC CMOS process and a 0.5V supply voltage. All MOS transistors are designed to operate in a weak inversion region in order to achieve low power consumption. Parameter x is set to 2/7 in the proposed OTA to achieve an equitable phase margin and transconductance enhancement. The transistor sizing for the FC, RFC, and TRFC OTAs is shown in Table 4.1. The AC response of the load capacitor CL = 30 pF and a biassing current of 5uA is shown in Figure 4.3. The large signal transient response for 250mVpp and a 50KHz step input is shown in Figure 4.4. The noise spectral density achieved by the RFC and TRFC is shown in Figure 4.5.

The FC, RFC, and TRFC OTA performance parameters are summarised in Table 4.2. In comparison to the FC OTA, the proposed TRFC OTA achieves a gain of 13.7dB and a gain of approximately 520 percent in the GBW. This demonstrates that the transconductance has increased. As expected, the reduced transconductance of transistors M3b and M4b results in a 16.730 phase margin degradation in the TRFC OTA. For an identical load capacitor and biassing current, the TRFC OTA has an SR that is 1.34 times larger than the RFC OTA. This results in a significant improvement in the TRFC OTA's settling time. However, as previously stated, the TRFC OTA has a higher equivalent input noise than the RFC due to the recycling current mirror's increased gain factor.

The transconductance is varied in Figure 4.6 by sweeping a voltage source from -50mV to 50mV. Vb = 50mV exhibits a minimum transconductance of 6.03uS and a maximum transconductance of 70uS. Thus, for varying values of Vb, the transconductance varies approximately 11 times from its minimum value. Thus, it can be seen that the proposed OTA can be easily converted to a tunable OTA only if the floating voltage source circuit used has a low output impedance. Table 4.3 illustrates how PVT variation affects OTA performance. To demonstrate how feasible the proposed TRFC OTA is, Table 4.4 summarises the performance parameters of the proposed TRFC OTA in comparison to other recently published low power OTA structures.

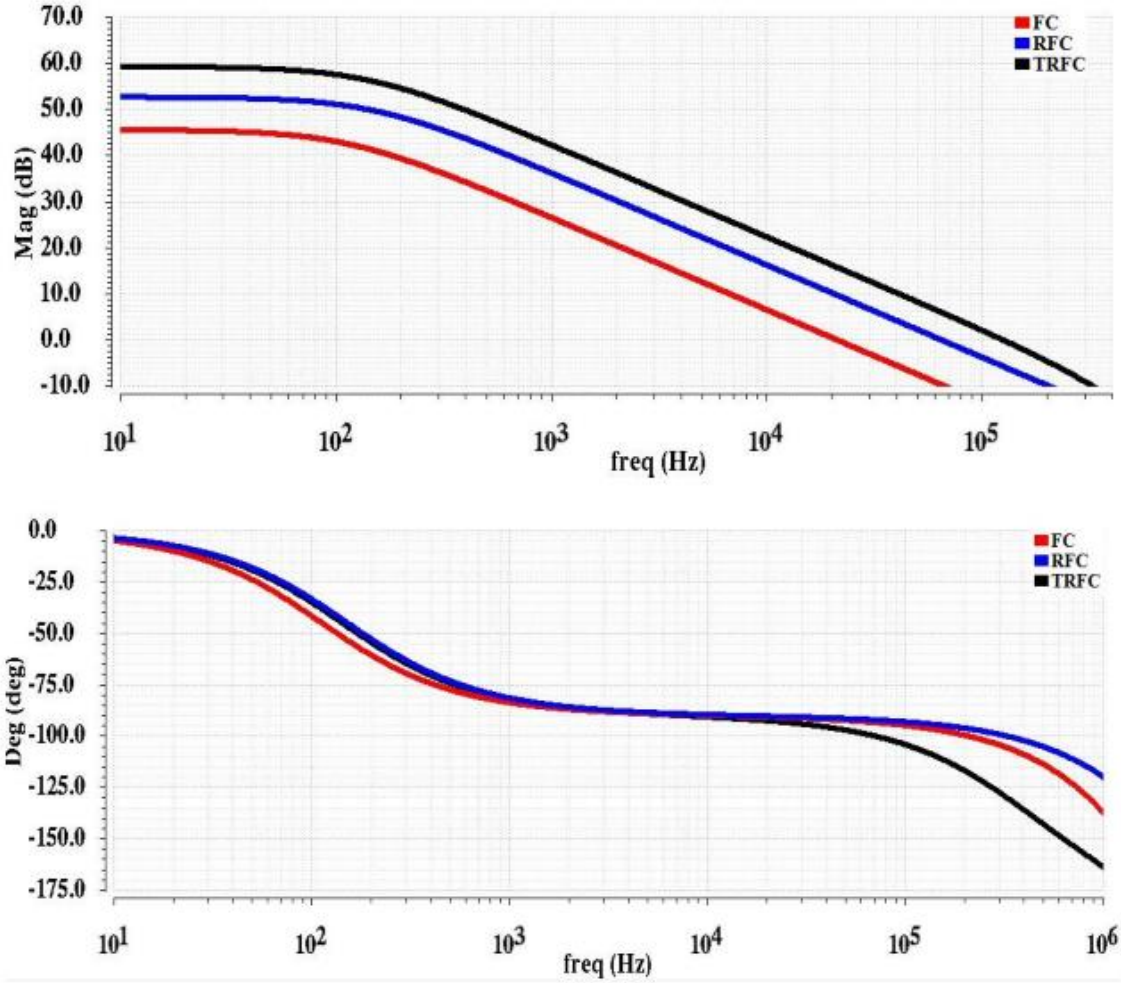

Figure 4.3. AC response of FC, RFC and the proposed TRFC OTA

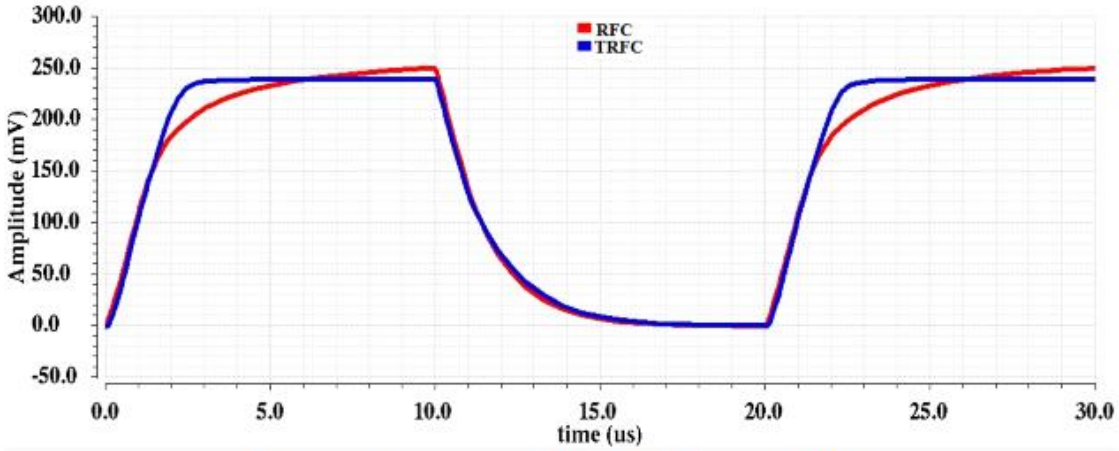

Figure 4.4. Large signal behavior of RFC and the proposed TRFC OTA

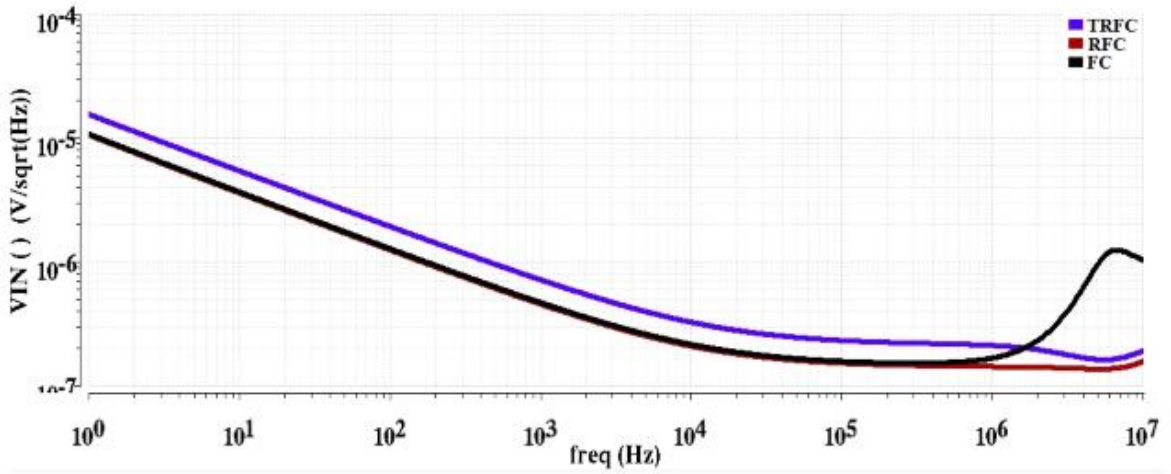

Figure 4.5. Noise spectral density of FC, RFC and proposed TRFC OTA

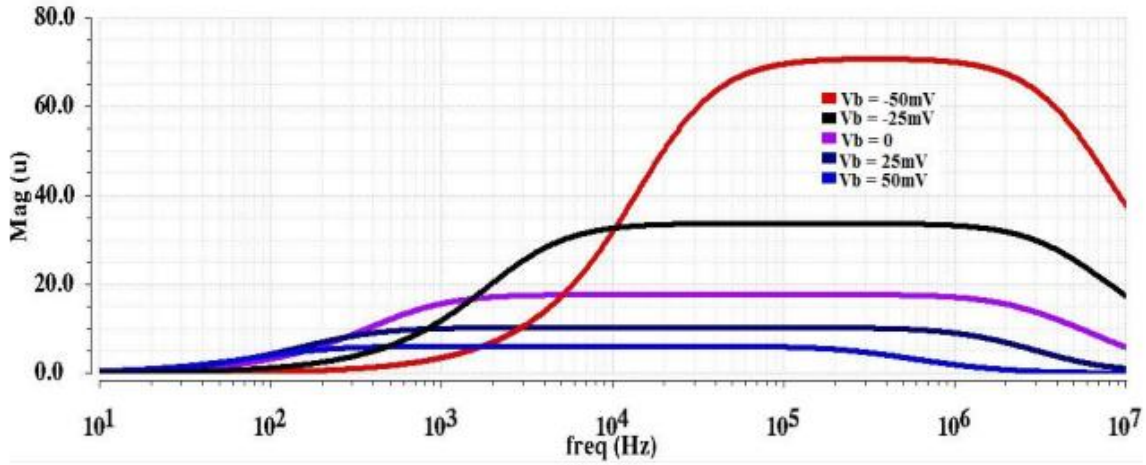

Figure 4.6 Transconductance variation by sweeping Vb

Table 4.1. Aspect ratio for FC, RFC and TRFC OTA

FC				RFC / TRFC			
MOS	W/L (um)	MOS	W/L (um)	MOS	W/L (um)	MOS	W/L (um)
M0	128 / 0.5	M5, M6	16 / 0.18	M0	128 / 0.5	M5, M6	16 / 0.18
M1, M2	128 / 0.36	M7, M8	64 / 0.18	M1a, M1b	64 / 0.36	M7, M8	64 / 0.18
M3, M4	32 / 0.5	M9, M10	64 / 0.5	M2a, M2b	64 / 0.36	M9, M10	64 / 0.5
				M3a, M4a	24 / 0.5	M11, M12	8 / 0.18
				M3b, M4b	8 / 0.5	MB	64 / 0.18

Table 4.2 Simulation summary for FC, RFC and the proposed TRFC OTA

Parameter	FC	RFC	TRFC
Technology	180	180	180
Supply Voltage	0.5	0.5	0.5
CL (pF)	30	30	30
Gain (dB)	45.50	51.99	60.05
GBW (KHz)	21.35	65.16	131.28
SR (V/us)	0.045	0.095	0.128
Phase Margin (degree)	89.29	83.55	72.56
Input noise @ 10 Hz [uV/sqrt(Hz)]	4.17	3.72	4.85
CMRR (dB)	39.03	52.83	66.46
PSRR+ (dB)	43.22	91.42	96.08
PSRR- (dB)	42.85	53.62	60.48
Offset Voltage (V)	0.21	0.0229	0.0408
FoM1 [KHz.pF/uA]	128.1	390.96	787.68
FoM2 [V/us .pF/mA)	270	570	768
Area (um2)	300.08	303.68	315.02

FoM1 = GBW x Load capacitor / Biasing current and

FoM2 = Slew Rate x Load capacitor / Biasing current

Table 4.3: Impact of PVT on the performance parameters of TRFC OTA

Parameter	Supply voltage		Process		Temperature Variation		
	550mV	450mV	FF	SS	-100	00	400
Gain (dB)	42.30	46	70.57	45.54	58.49	58.89	59.03
GBW (MHz)	0.256	0.0013	1.43	0.147	26.36	41.37	218.89
SR (V/us)	0.16	0.051	0.79	0.0035	0.053	0.067	0.15
Phase Margin (Deg)	87.58	85.6	84	16.25	77.49	76.72	69.82
1% Settling Time (us)	59.93	59.96	59.66	59.84	59.97	59.98	59.98

Table 4.4: Comparison of TRFC with recently published OTA structures

Parameter	[76]	[86]	[60]	[85]	[15]	TRFC OTA
Technology (nm)	50	180	180	180	180	180
Supply Voltage	0.5	0.6	0.3	0.5	0.5	0.5
CL (pF)	20	15	15	15	20	30
Gain (dB)	74	82	106.3	67.8	47.7	59.20
GBW (MHz)	4.8	0.0191	0.033	0.00326	17.8	0. 131
SR (V/us)	3.4	0.012	0.028	0.00072	9	0.128
Phase Margin (Deg.)	49	60	102.4	68.9	60	72.56
Input referred noise [uV/sqrt(Hz)]	0.118 @ 10KHz	0.152 @1KHz	0.1500 @1KHz	0.56 @ 1KHz	0.080 @1MHz	4.85 @ 10Hz
PSRR+ (dB)	81	--	104.8	--	58	96.08
PSRR- (dB)	--	--	124.3	--	58	60.48
CMRR (dB)	106	130.2	126.6	--	138	66.46
Power (W)	100u	400n	370n	26n	60u	23.8u
Transconductance Tuning Range (uS)	--	--	--	--	--	6.03 to 70
FoM1 [KHz.pF/uW]	960	716.25	1365	1881	5934	166
FoM2 [V/ms. pF/uW]	680	450	1135	410	3000	162

CONCLUSION:

The following summarises the chapter's major points:

- The proposed modification to the RFC OTA's input stage significantly improves the performance of the conventional RFC OTA.
- The enhancement is accomplished without impairing the existing RFC OTA circuit's power budget.
- The measurement result confirms the transconductance enhancement, with an increase of 520 percent and 13.7 dB in GBW and DC gain over the conventional FC OTA, respectively.
- A simulation result demonstrates that the proposed OTA is capable of operating as a tunable OTA by varying the voltage source.
- Further improvement in transconductance is constrained by phase margin degradation. Adopting a suitable phase compensation scheme, as proposed in [56, 104], can increase transconductance while incurring a cost in terms of area and power.

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