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NOVEL BACK-BIAS ASSIST TECHNIQUE FOR DESIGN OF FULLY DEPLETED SILICON-ON-INSULATOR BASED SRAM BIT CELL

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ABSTRACT: Nowadays the power saving methods has become essential for modern day digital systems. The SRAM (Static Random Access Memory) is one of the major parts of cache utilized in such systems; hence its reduction of consumption of power has been researched since many years. In recent times, convincing reduction of power is attained in SRAM cell with minimal criteria path delay by the sleep transistor method; however it degrades the SRAM cell logic state as well as its performance. A Novel Back-Bias Assist Technique for Design of Fully Depleted Silicon-on-Insulator (FDSOI) Based SRAM Bit cell is presented in this paper. FDSOI device based SRAM design is implemented here that will eliminate the requirements of sleep transistor for power consumption reduction. For this SRAM design, architecture with the local back-plane for the top-tier transistor is utilized to enable the local back-bias assist methods with no penalty of area and the capabilities for routing two extra row wise signals over individual back-planes. This will reduce the total complexity and power gating memory designs overheads. The SRAM configuration performance metrics will be evaluated and compared. The experimental data will be extracted from 14 nm planar FDSOI. The simulation results indicate that this technique reduces the bitline capacitance, improvements in write/read access time and reduces the minimum operating voltage V_{min}.

KEY WORDS: SRAM, Sleep Transistor Technique, power consumption, FDSOI, Back-Bias Assist Technique.

I. INTRODUCTION

The scaling technology imposes the variation issues when it is beyond 32 nm. The issues are manifested as fluctuations in consumption of power, stability and degradation of maximum speed.

These variations are classified as two different groups namely: process and environmental. The process variations are the consequence of imperfections during development process and are translated as transistors non-deterministic behaviour. The SRAM is one of the integral segments of SoC (Syste-on-Chip) design. In portable electronic devices, the SoCs have certain requirements such as high speed and less power operation modes. In low power operation modes, the SRAM in a SoC might be operated at lower voltages whereas in high speed operation it operates at high voltages [1]. Because of the increasing device variability with every scaling technology, the SRAM low voltage operations have been become more challenging. Meanwhile new multi-core processor architectures are demanding more on-chip caches in order to share the data effectively across parallel processing units. Mainly such memories are designed with the SRAMs as they occupy the greatest part in chip area and the SRAM cell has great significance, as one of their main units, the SRAM is

scaled with minimum dimensions. Moreover the fluctuations of parameters have significant influence over circuits which can rely perfectly on the pairs of matched transistor and if SRAM cells smaller dimensions are added to the previous statements then it is clear that why process variation has significant importance over them [2].

In SRAM design the most vital concerns are reliable write and read operations because of the 6T (6 Transistors) symmetry and straight forwardness. The SRAM cell circuit area is very effective. But in 6T cell two-bit line structure the bit lines can't be separated electrically from the storage nodes during the operations of write as well as read [3]. However, during read operation the cell might be highly vulnerable to noise. A storage node voltage with 0 may rise to higher voltages than ground because of the voltage division across the access and PD (Pull Down) transistors, at the center of the pre-charge Bit-Lines (BL & BLB) and SRAM cell ground terminal. By reading the wrong value, this case can be end generally it is called as read upset [4].

One of the most effective ways for achieving the functionalities of low voltage is using circuit methods for assisting write or read stability operation [5]. Word-line under-drive is the more commonly utilized read stability assist method whereas various write-assistant methods have been suggested that includes word-line boost, Gnd (Ground) raising, Vdd lowering and negative bit-line approach. The major disadvantages of these approaches are SRAM dynamic power and cost on area because of the extra components of circuit [6]. Meanwhile a limited gain is there while reducing the Vmin which is the minimal functional voltage. The requirements of portable devices for low consumption of power and higher speed performance have highlighted the requirement of circuit operations on wider range of Vdd (supply voltages) for the maximization of energy efficiency to the given performance requirements [7]. Though, in deeply scaled technologies, the SRAM can be prevented for obtaining as low as Vdd_{min} as logic by the increased variability. Due to their less leakage currents, reduced RDF (Random Dopant Fluctuations) and excellent short-channel electrostatic channel, the un-doped thin-film planar FDSOI devices have been investigated as the alternatives to bulk CMOS (Complementary Metal Oxide Semiconductor) for 28nm node and beyond it [8].

II. LITERATURE SURVEY

Jae-Won Jang et. al. [9] presented an 8T (8 Transistor) SRAM PUF (Physical Un-clonable Function) with back-to-back PMOS (P-channel Metal Oxide Semisnoductor) latches for improving the robustness by 4 times. The less power 7T (7 Transistor) SRAM is presented with the employed MTJ (Magnetic Tunnel Junction) devices for enhancing the robustness (from 2.3X to 20X) by reducing the area overhead and leakage power. The PUF function is a costly security primitive used for addressing the hardware attacks like cloning, IP (Intellectual Property) violation and impersonation. J. D. Black, et al. [10], presented SRAM PUF where single-event Physical mechanisms effects lead to the charge collection of multiple nodes or charge sharing is summarized and reviewed. From the historical overview of given circuit responses, it has observed that it majorly concentrated over memory circuits. With the single-node upset methodologies the memory devices might be used for exhibiting various cell upsets. With spatially redundant logic, the memory devices might be used for upset if the charge on multiple circuit nodes is collected in a latch. Impacts on characterization of such effects in different models are discussed; hence a ground-based testing has been suggested.

Arora N et al. [11] presented a design strategy of fully differential less power 10T (10 Transistor) SRAM bit cell where the tail transistor is connected in series. This device gate electrode is controlled with XOR gate input and its inputs might be tapped from WWL (Write Word Line) to RWL (Read Word Line) and control signals are taken from RWL and WWL drivers. The tail transistor and XOR gate can be shared through all of the cells in a row. Here tail transistor might be upsized relatively to sink the currents from the cells of a row. Shilpi Birla1 et al. [12] has analyzed an 8T SRAM cell at 65nm technology. Actually this technology is presented to a sub-threshold SRAM design and optimized for performance and functionality on larger voltage ranges. The write operation could be done by WBLX (Word Bit Line) port, WBL (Word Bit Line) and WWL while single ended read operation might be conducted by RBL (Read Bit Line) and RWL ports. At every read

cycle end, the RBL might be pre-charged and keeps pre-charged in write cycle. Morrison et. al., [13] has presented an SRAM design by the reversible circuit. If the output of each gate is redundant then it is called as garbage output. While designing the reversible circuit, the major challenge is garbage output reduction.

Kursun V. et al. [14] presented a 9T (9 Transistor) SRAM. Here the write operation appears as same as 6T SRAM cell. Whereas the reading appears separately via Access transistors which are controlled by RWL signal which is high. But this approach has higher bit line capacitance issue with more number of pass transistors over bit line. P. E. Dodd and L. W. Massengill et. al., [15] demonstrated single event upset "basic mechanisms and modelling in digital microelectronics. This work is a single-event effects historical overview in terrestrial and space systems and upset strategies in DRAMs (Dynamic Random Access Memory), SRAMs are demonstrated in detail. Methods to reduce the upset of single event are discussed and techniques to predict the device and single event responses of circuit by computer simulations. The impacts of trending technologies on the susceptibility of single-event and future concern areas have been explored.

III. NOVEL BACK-BIAS ASSIST TECHNIQUE FOR DESIGN OF FDSOI BASED SRAM BIT CELL

Mainly this work will be focused on SRAM back-bias assist methods while utilizing the FDSOI unique features. The FDSOI is utilized for designing the bit cell circuit of SRAM. The sleep transistors are eliminated by this design model and this will lead to area overhead reduction and SRAM bit-cell performance improvement. Here the idea is exploiting the BG (Back Gate) bias in FDSOI for getting the desired V_{TH} (Threshold voltages) dynamically with no sleep transistors. However additional transistors do not need for power gating and there is a need of set the low and high V_{TH} values dynamically in same FDSOI device. In read and write operation less V_{TH} value will be preferred for high gate drive. While high V_{TH} value is preferred during hold mode for decreasing standby leakage power.

3.1 FDSOI

The FDSOI device is viewed as two MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) (front & back) which shares the same drain, source and body region and is illustrated in Fig. 1.

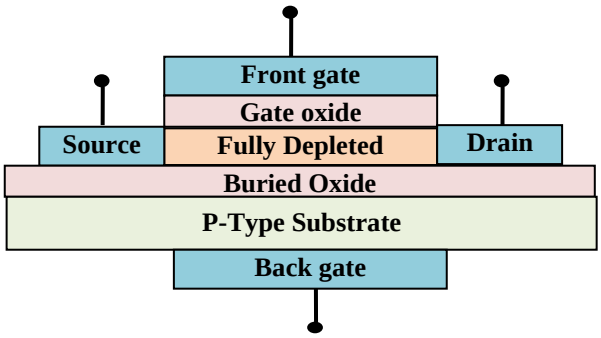

Fig. 1: FDSOI MOSFET Device

An extra BG contact might be given under the substrate. The charge in silicon channels is controlled by the two gates of the device. In FDSOI, usually the thickness of silicon film will be less than or equal to half of the depletion width of bulk device. In addition the device V_{TH} and drain current values will be subjective to the thickness of film. The thin films need to have greater control on device performance since the FDSOI devices V_{TH} will be sensitive to the changes in SOI Tsi (the Thickness of silicon film). Further thin SOI film is needed for minimization of short-channel effects in SOI MOSFETs. The FDSOI device surface potentials at front and back interfaces might be coupled tightly with others and coupled capacitively with front-gate and the substrate by buried oxide and front-gate oxide. The FDSOI device V_{TH} (Threshold voltage) is depends on the FDSOI BG voltage. The FDSOI V_{TH} is expressed as:

$$V_{TH} = V_{FB\_F} + 2\Phi_B - \frac{Q_B}{2C_{OX}} - (V_{BG} - V_{FB\_B} - 2\Phi_B + \frac{Q_B}{2C_{BOX}}) \times \frac{C_{SI}C_{BOX}}{C_{OX}(C_{SI}+C_{BOX})}$$ -- (1)

$$Q_B = -qN_ATT_{si} \text{ (or) } +qN_DTT_{si}$$ ------ (2)

Where V_{FG} is the voltage of Front Gate and V_{BG} is the voltage of BG. V_{FB_F} is front gate Flat-Band voltage and V_{FB_B} is BG Flat-bBand voltages. C_{OX} is the front and BG oxide. C_{BOX} is the film capacitance of buried oxide and C_{SI} is the depleted silicon film capacitance. $Q_B$indicates the charge density of area in depleted Si (Silicon) film.

3.2 Back-Bias Assist Technique

The planar CMOS devices would be fabricated featuring 20 nm minimum gate length, 6nm-thin channels, 90nm Contacted Poly Pitch, 0.078μm2 SRAM minimum area, SiGeB (Silicon Germanium Boron) / SiP (Silicon Potassium) in-situ doped source/drain and 64nm Metal Pitch. All the HC/HD (High Density/High Current) transistors i.e. PU (Pull-Up) pMOS (p-channel Metal Oxide Semiconductor) and PG (Pass-Gate) and PD nMOS (p-channel Metal Oxide Semiconductor) will be built over silicon channel with a single p-doped well and a single gate metal. Experimentally the SRAM sensitivity vs. back bias will be characterized. The FDSOI 6T SRAMs will be built over single PW (P-Well) which is biased negatively to save leakage or biased positively for performance improvement.

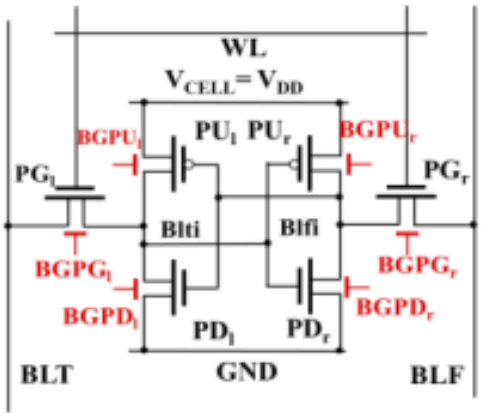

Fig. 2: Schematic of Back-bias assist FDSOI SRAM

The BG bias utilization may impact the margins of cell that should be co-optimized with leakage and performance. The PW biasing is also utilized for adjusting the SRAM arrays read-write balance, tightening the total distribution of V_{min}. The negative PW biasing will result less pMOS V_t and high nMOS Vt that will improve the read stability of bit cell at write margin expense. As the well would be shared among all the devices in an analyzed bitcell, then $V_{well}<0$ will improve the strength ratio of PG/PU and increase the write current (the PG drive governs it). Thereby the back biasing is utilized for assisting the write ($V_{well}>0$) as well as read ($V_{well}<0$) operations.

IV. RESULT ANALYSIS

The design kit and FDSOI Spice model are built while utilizing the electrical parameter characteristics of CoolCube™ low- temperature procedure. The detailed study about independent back-bias influence for PU/PG/PD demonstrated that the PU V_{TH} should be lessen (VB_{pu} <0) to all the FoM (Figure of Merit) that can't be accomplished simply by the gate-first FDSOI procedure with a Si channel. This will be done by the dedicated PU back plane with an applied constant bias (VB_{pu}=-0.8V) in all modes of operation. In addition, the threshold voltage of PD (or PG) is modulated dynamically as per the operation of SRAM for improving

the margins as well as currents. The three different assist modes (with different $VB_{pd,}$ VB_{pu}, VB_{pg}) will be chosen to write (A1), read stability (A2) and read time (A3) assist. The following figure shows the performance of novel back-bias assist technique on three SRAM operation modes. It is observed that the yields of versatile assist are+28% I_{write} with A1, +28% I_{read} with A3 at VDD=0.8V, +23% WNM (Write Noise Margin), +4% SNM (Static Noise Margin) and V_{well}= ± V_{dd}/GND vs. reference configurations at 0v with single back-plane. In addition the gains might be pronounced at low V_{dd} this will lead to 60mV V_{min} reduction with A2.

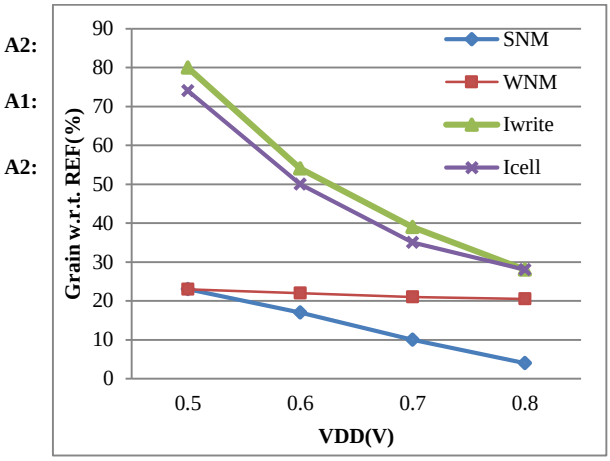

Fig. 3: Performance of novel back-bias assist technique on SRAM operation modes

The relevant layout (same for A1-A2-A3) is designed, that connects two local back planes groups (to-a-bit-cell) for PG and PD via internal bias with no penalty of area. Generally the back plane lines which are parallel to BLs will distribute the static PU bias. These two dynamic signals would be routed in WL direction with the height of SRAM (while in planar technologies, the wells are generally in BL direction). Hence the back biasing will allow boosting a chosen row from top-tier with no other rows distribution.

The two most significant metrics of SRAM in terms of its robustness and reliability are write ability and read stability. Usually the SRAM robustness and reliability are investigated by widely accepted N-curve technique. This method is utilized for measuring the write ability and determining the stability of reading. The SRAM cell stability is represented as current by N-curve. Initially the presented design is set for holding "0". The DC noise source (I_{IN}) will be connected to the Q_B of SRAM cell. Both these bit-lines BLB (Bit Line Bar) and BL (Bit Line) would be clamped to V_{dd}. Next the DC (Direct Current) sweep would be conducted over Q_B for obtaining the current waveforms. The current curve crosses the 0 at A, B &C which is illustrated in Fig. 4.

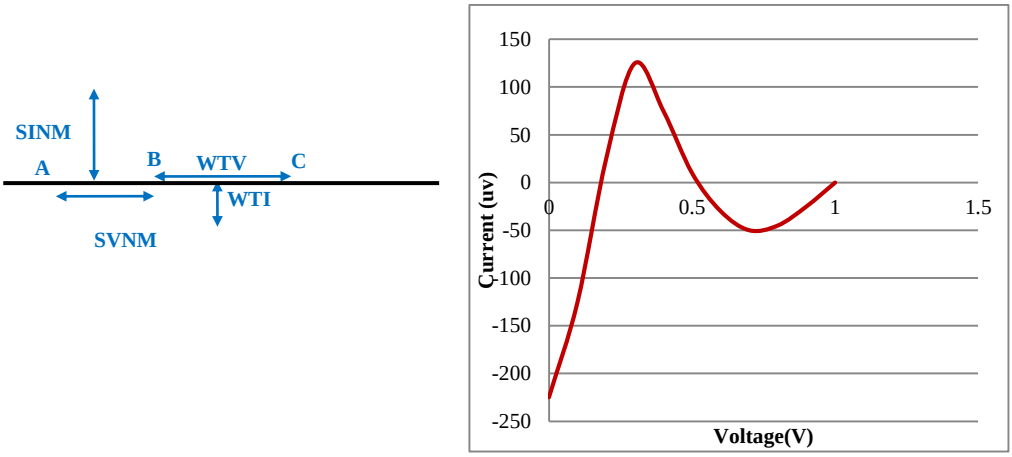

Fig. 4: N-curve analysis of FDSOI SRAM cell

Here the ability of write is shown between C and B. The voltage difference between B and C is referred as WTV (Write Trip Voltage). The WTV is the voltage and is needed for changing the cell data. The WTI (Write Trip Current) is the negative peak current differences between B & C. The WTI is a cell current margin that will change the stored data in storage node. In the same way, the read stability is represented between A and B. The voltage difference between B and A is Static Voltage Noise Margin (SVNM). The SVNM is a highest tolerable DC noise voltage before flipping the cell content. SVNM is the current peak between A & B. This is the highest current which is injected in a SRAM cell while not flipping the cell data.

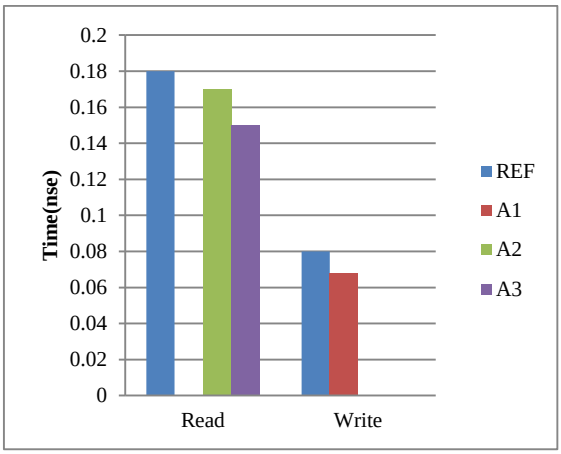

Fig. 5: Read/write time of SRAM cell

For the evaluation of capacitive gain which is offered by the local plane compared to continuous plane (or single well in planar), backend parasitic are extracted.12/16% of read/write time improvement and 7% of BL capacitance is attained (at V_{dd} =0.8 V).

V. CONCLUSION

Novel back-bias assist technique for design of FDSOI based SRAM bit cell was implemented in this research. At first, FDSOI device based SRAM design is presented that eliminates the sleep transistors requirement for power consumption reduction. Further this reduces the total overheads and complexity of power gating memory design. Then back bias assist technique is used in this to design FDSOI based SRAM cell which might reduce the Vmin as well as access time of read/write operation. Since the variability has become an vital reason for WNM and SNM in the SRAM cell, this FDSOI based SRAM enhances the stability and performance while tuning the PD and PU transistors threshold voltage. From result analysis it can be illustrate that the FDSOI based SRAM cell significantly improved the performance of read and write operating by finding the better SNM and WNM. From the result it is seen that the SRAM cell has consumed low energy and writes quicker than reference model design.

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