SOLAR POWERED ELECTRIC VEHICLE WITH 53 LEVEL MULTILEVEL INVERTER FOR THREE PHASE INDUCTION MOTOR DRIVE

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Abstract: Multilevel inverters (MLIs) can be utilised in a inclusive range of applications, including Electric Vehicles (EV) and solar PV. This research presents a 53-level multilevel inverter structure for EVs that utilises a (SC) Switched Capacitor technique. The number of SC cells determines the number of levels in MLI design. The proposed structure is simple and straightforward in terms of implementation. There are fewer driving circuits as the number of active switches decrease. As a result, the MLI cost,size and number of devices are lowered. An Improved Incremental Conductance (INC-MPPT) and a Single Input and Multiple Output converter (SIMO) boosts the DC link voltage using solar panels to offer a constant DC voltage and THD also reduces the multilevel inverter output voltage. A simulation model is built in MATLAB.

Keywords: Electric Vehicles (EV). Multilevel inverters (MLIs), Improved Incremental Conductance MPPT (INC-MPPT), THD

I.INTRODUCTION

Conventional inverters are struggling to keep up with the demand for high-quality energy in industrial applications and solar PV installations. High quality energy may be produced by using multilayer inverters, which are becoming more and more popular. Using this technique may lead to a decreased number of devices, a lower switching frequency, less DVT stress, and less harmonic distortions. [1]. There are many fewer components in contemporary inverter designs compared to prior designs, such as the flying capacitor, Neutral Point Clamp (NPC) and Cascaded H-bridge (CHB), The additional layers of the MLI may be directly responsible for increasing the circuit's complexity and price [2]. The capacitor voltage balancing in the FC and NPC MLIs is limited to five levels and cannot be cascaded. However, since the o/p voltage is only half as high as the input voltage, this raises switching frequency and increases power consumption. [3]. Alternate network topologies have been suggested for MLI's numerous components, depending on which tiers are encountering problems. The numbers 7 and 8 are sequential. Other MLI topologies are discussed in [4] in reports that do not fall into one of the three conventional categories. Sub multilevel converter concepts presented are critical. As mentioned in [5], a basic level structure requires a significant number of direct current voltages. [6] and [7] describe the linked inductor-based topologies. Even though these structures are simple, they are challenging to expand to higher levels. The output voltage levels [8] and [9] of new MLI topologies based on SC boost methods are limited to 5, 7, and 13. An even more complex MLI topology than that shown in [10] is possible. Each extra switch or device requires greater resources in terms of both money and floor area. Using a multilevel converter and a complete bridge, illustrates a novel SC MLI design. Because of the rising complexity of the controls and the growing number of devices, the SC-based MLI architecture is no longer viable. The highfrequency output is necessary since the carrier frequency is utilized to transition frequencies. It is probable to

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expand the number of output voltage levels by using SC's partial charging approach. Partial charging is a significant challenge in terms of control complexity. It's not a simple effort to create a SC-based MLI [11] that can produce high frequencies with low harmonics and decent efficiency. Because of its smaller size and less weight, high-frequency output is well-suited for usage in electric vehicles. [12] The two types of photovoltaic panels are those that use the sun's power to generate electricity and those that convert that power into direct current (DC). To provide power to the converter, a DC connection is required . Solar PV production cannot be forecast because of changes in temperature and irradiance. The maximum power point tracking (MPPT) of a PV module is necessary to maximize the amount of energy that can be harvested from the module. Use of a DC-DC converter is necessary for managing maximum power in a system using MPPT. PV-fed inverters [13] must be regulated to maintain a steady DC voltage output. When using stand-alone PV systems, the PI controller is utilized to choose the correct duty cycle for the converter. Many topologies [14] [15] have been suggested to address the problem of MPPT control of the DC-DC converter in a standalone solar system. Artificial intelligence, practical swarm optimization, fuzzy algorithms, and evolutionary algorithms have recently been used to make automatic voltage adjustment conceivable. In order to pick an MPPT method, it is necessary to weigh the advantages and disadvantages of various options. perturb and observation (P&O), Hill climbing (HC), and other MPPT techniques [16] are popular because of their ease of usage. It is impossible to extract the global MPP (GMPP) using traditional approaches, such as fuzzy, P&O, and INC algorithms, in partial-shade conditions. The use of MLI with a DC connection and MPPT to modulate outputs under continuous solar irradiation or load management has been documented in many studies. An MPPT of a PV panel regulates the panel's energy output to run at its maximum power point (MPP). Temperature and sun irradiation vary throughout the day depending on the season and the weather. This implies that if you want to have the most impact, you need to keep an eye on each of these variables at all times. A single DC-DC boost converter and many output DC-DC converters are used in this study to create a solar PV system. There are 53 speeds available for the inverter to choose from. The suggested system maximizes the maximum output of the solar panels using improved incremental conductance-powered MPPT. Before it reaches the 53-level inverter, the voltage is raised using a single i/p multiple o/p boost converter. The number of devices, power losses, efficiency, and total harmonic distortion (THD) are all taken into account while evaluating and comparing different MLI topologies (THD). MATLAB/Simulink and an experimental hardware setup are required to test the built system.

II. EXISTING SYSTEM

The below figure.1 indicate the single phase 53 level-MLI which is fed by solr PV. The system contains the three level DC/DC boost converter, solar PV and 53 level inverter. the arrangement is indicated in figure.1 The solar PV conneted to 53-level inverter via DC/DC boost converter. The boost converter can be controller by MPPT technquie namely P & O MPPT. And the MLI is controller by PD-PWM technquie. Because of using P and O MPPT tracking point of power is higher.



Fig1. Single phase overall 53 level – multilevel inverter system.

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III. PROPOSED SYSTEM

The below figure.2 shows PV connected 53level- Multilevel Inverter with phase disposition pulse width modulation for electric vehicle. The system contains Solar PV, DC-DC converter, three phase 53 level inverter topology and induction motor. The DC-DC boost converter controlled by Improved incremental conductance MPPT and three phase 53 level inverters controlled by PD-PWM technique the arrangement is shown in figure 2. The induction motor is fed by proposed 53level-MLI inverter.



Fig .2 Proposed PV connected 53-Level Multilevel Inverter for electric vehicle

1) MODELLING OF SOALR PV

The PV cell contains parallel resistance and series resistance RSH and RSE, understood to be an analogous circuit shown in figure.1. Ipv and Vpv are the o/p current and voltgae of the solar cell, correspondingly. These are grew from the parallel and series connection of mulitple soalr modules specified in eqn (1),

$$I_{PV} = \left\{ I_{Ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_{SE}I_{PV})}{N_{SE}AKT}\right) - 1 \right] - \frac{(V_{PV} + R_{SE}I_{PV})}{N_{SE}R_{SH}} \right\}$$
(1)

where NSH and NSE are Number of PV cells in parallel and series correspondingly. The parallel resistance is represented by RH, the series resistance is represented by RSE, A semiconductor device's ideality factor. For the sake of clarity, we will refer to the temperature as T. In the equation, Ip is the produced current, and it is depending on the irradiations and temperature levels (2)

$$I_P = [I_{SK-STM} + K_i(T - T_{STM})] - \left(\frac{G}{G_{STM}}\right)$$
(2)

where ISK–STM I standard testing cases (STM) short-circuited current, Ki is SCC coefficient, G (W/m2) is cell irradiance, GSTM (1000W/m2) is the STM is irradiance, and the TSTM is temperature of cell.

$$I_0 = \left\{ \frac{I_{SK-STM} + K_i(T - T_{STM})}{\exp[(V_{OK-STM} + K_{OV}(T - T_{SKC})/AV_{sh})]} \right\}$$
(3)

where VOK-STM is standard testing case open-circuited voltage, KOV represents voltage coefficient of open-circuit, VSth is thermal voltage of solar cell.

$$P_{PV} = V_{PV} \times N_{SH} \left(I_{Ph} - I_O \exp\left(\frac{qV_{PV}}{N_{SE}AKT}\right) - \left(\frac{V_{PV}}{N_{SE}}\right) \right)$$
(4)

2) IRRADIANCE AND TEMPERATURE EFFECT

As the environment changes, so does the production of solar panels. irradiance limitations impact the sun's I-V/P-V characteristics at different angles of incidence. As long as the amplitude of the voltage pulses VPV changes, IPV remains constant. Temperature change in a solar photovoltaic system is influenced by three factors: The ultraviolet wavelength, which is worn on the solar cell, helped to eliminate heat during PV

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operation by increasing the intensity of the sunbeam. It is possible to measure VOC and ISC at different irradiances using the formulas (5) and (6).

$$V_{OC} = V'_{OC} + a_2(T - T') - (I_{SC} - I'_{SC})R_{SE}$$
(5)
$$I_{SC} = I'_{SC} {G/_{G'}} + a_1(T - T')$$
(6)

The temperature coefficients A1 and A2 from the previous equations are the PV cells. V0 OC and I0 SC are calculated using G' and T0 as the reference standards, respectively. The output voltage and current may be affected by a variety of external factors. In the course of a solar PV installation, its production may be maximized. MPPT systems monitor irradiance and temperature to ensure a steady output voltage.

3) PARTIAL SHADING EFFECT

An MPPT technique that tries to maximize power production has an extra obstacle when a solar panel is partially shaded. A partial shadow may be cast by mists, trees, buildings, and other natural occurrences. The photocurrent Iph decreases with decreasing insolation, according to equation (2). When a PV module's cells are linked in series, the total current flowing over the module is the same. For this reason, the darkened cell degrades and becomes a burden rather than an energy source.

4)MPPT CONTROLLER

IMPROVED INCREMENTAL CONDUCTANCE MPPT FOR BOOST CONVERTER

Increasing the electrical conductivity Control of the boost converter occurs through MPPT here. Despite its intricacy, the fact that it can work in a wide range of atmospheric conditions says a lot about its adaptability. The first flowchart employs PV panel voltage and current data to compute incremental conductance, which is subsequently utilized in Figure.3 to calculate incremental conductance. With a new algorithm, the constraints of the InC approach have been reduced. This estimate simplifies the dp/dv difference calculation.

$$\frac{dp}{di} = \frac{P(k) - P(k-1)}{V(k) - V(k-1)} \quad (7)$$

When paired with a CV algorithm, the InC technique is limited in its search area since it can only estimate the MPP voltage [28, [29]]. A PV panel's output voltage (MPP) is directly related to the CV algorithm's output voltage (open circuit voltage) (OCV). It is considered normal to have a VMPP/Voc ratio of roughly 76%. P-V characteristic is divided into three unique zones using modified InC algorithm, with zone 1 covering 0–70% of the Voc and zone 2 covering 70–80% of the VOC. Zone 3 covers 80–100% of the VOC using modified InC algorithm. This section also includes the MPP. The enhanced InC algorithm just has to search for the MPP in area 2, which has a Voc of 70% to 80%, to provide the best results possible. Thus, this is the end outcome

$$V_{ref} = (70\% - 80\%)V_{oc} = (V_1 - V_2) \quad (8)$$

In the new InC method, MPPT is temporarily decreased to zero in order to monitor PV panel open circuit voltage. For the first time ever, you can see how this new InC algorithm works by looking at its diagram. The solar PV panel's ST and MPPT are used in conjunction to regulate the whole atmosphere.



Fig.3 Flow chart of improved incremental conductance MPPT algorithm

5)DC/DC BOOST CONVERTER

Figure.1 depicts a DC-DC boost converter with a single input and several outputs that is connected to the PV panels and the suggested inverter. This converter produces a 4:1:3:9 ratio of three independent dc sources. One solar PV feeds the converter, which eliminates both uneven voltage and step size fluctuations due to various climatic circumstances. The inductance can be determine using the following equation:

$$L = \left(\frac{mV_{dc}}{4af_s l_r}\right) \tag{9}$$

This converter produces a 4:1:3:9 ratio of three independent dc sources. One solar PV feeds the converter, which eliminates both uneven voltage and step size fluctuations due to various climatic circumstances. The inductance can be defined by using the following equation:

$$C = \left(\frac{DI_{dc}}{V_{dc}rf_s \times 0.5}\right) \tag{10}$$

where Vdc is the DC voltage, m is represents modulation index, and fs represents the frequency of switching, Ir represents ripple currents, overloading factor is represented by a which is typically 1.25. The formula for calculating capacitance is as follows:

$$D = \left(\frac{V_0}{V_0 + V_{dc}}\right) \tag{11}$$

where Idc represents the dc current, switching frequency represents by fs, ripple voltage represented by Vr, dc voltage represented by Vdc, duty cycle represented by D. The following relationship can be used to calculate the converter's duty cycle:

6) SINGLE PHASE 53-LEVEL MLI

An MLI with 53 levels is depicted in FIGURE 5.9 by connecting three SC units with an even fewer number of components. 3 asymmetric DC sources along with no inductors form the basis of the proposed MLI topology. DC sources of different voltage levels generate an uneven structure. This MLI topology reduces voltage stress, total standing voltage (TSV), weight factor, transient harmonic distortion (THD), switch count, component Copyrights @Kalahari Journals Vol. 7 No. 5 (May, 2022)

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count, and other power quality issues. This topology has a lower TSV than other topologies and is compared to them. Table-i shows the course of the current at the load through the switches, as well as the states of operation. Figure .3 shows a few modes of operation, as well as the switching pulses. TABLE-I shows the various modes of operation for the 53-level MLI that has been built. To achieve a maximum voltage of 400.4 volts in mode-1 operation of the circuit, the switches SE, S2, SA, S7, SD, S4, S5 turn on, producing a load current channel through which V1, VC1, V2, VC2, V3, and VC3 sources operate and generate the voltages of 15.4V, 15.4V, 46.2V, and 46.2V, respectively.



Fig 3. Single phase 53-Level ML



Fig.4 Operating modes of the single phase 53-Level multilevel inverter .

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Connecting 3 SC units with an even lesser number of components results in an MLI with 53 levels in FIGURE 4. The suggested MLI topology is based on three asymmetric DC sources without inductors. DC power sources with varying voltage levels provide an uneven structure. Voltage stress, total standing voltage (TSV), weight factor and transient harmonic distortion (THD) are reduced by this MLI structure. When compared to other topologies, this one has a lower TSV. The table-I displays the path of the load currents, as well as the states of operation, of the switches. Figure.4 depicts some operating modes, as well as the switching pulses that are used to control them. The 53-level MLI has been constructed, and the several operating modes are indicated in Table I. Mode-1 of operation in the circuit requires the switches SE and S2 to be turned on to produce a load current channel through which the V1, V2, VC2, V3, and VC3 sources operate and generate the voltages of 15.4V, 15.4V, 46.2V, and 46.2V, respectively; this is achieved by switching the switches SE and S2 on.

States	Load current path	Output Voltage (V)		
State-1	S _E , S ₂ , S _A , S ₇ , S _D , S ₄ , S ₅	$26V_{dc}$	$V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3}$	400.4
State-2	S _E , S ₂ , D ₁ , S ₇ , S _D , S ₄ , S ₅	$25V_{dc}$	$V_1+V_2+V_{C2}+V_3+V_{C3}$	385
State-3	S _E , S ₂ , S _B , S _A , D ₁ , S ₇ , S _D , S ₄ , S ₅	$24V_{dc}$	$V_2 + V_{C2} + V_3 + V_{C3}$	369.6
State-4	S _E , S ₂ , S _A , S ₇ , D ₂ , S ₄ , S ₅	23V _{dc}	$V_1 + V_{C1} + V_2 + V_3 + V_{C3}$	354.2
State-5	S _E , S ₂ , D ₁ , S ₇ , D ₂ , S ₄ , S ₅	$22V_{dc}$	$V_1 + V_2 + V_3 + V_{C3}$	338.8
State-6	S _E , S ₂ , S _B , S _A , D ₁ , S ₇ , D ₂ , S ₄ , S ₅	21V _{dc}	$V_2 + V_3 + V_{C3}$	323.4
State-7	S _E , S ₂ , S _A , S ₇ , S ₈ , S ₅	$20V_{dc}$	$V_1 + V_{C1} + V_3 + V_{C3}$	308
State-8	S _E , S ₂ , D ₁ , S ₇ , S ₈ , S ₅	$19V_{dc}$	$V_1 + V_3 + V_{C3}$	292.6
State-9	S _E , S ₂ , S ₃ , S ₄ , S ₅	18V _{dc}	$V_{3}+V_{C3}$	277.2
State-10	D ₃ , S ₂ , S _A , S ₇ , S _D , S ₄ , S ₅	17V _{dc}	$V_1+V_{C1}+V_2+V_{C2}+V_3$	261.8
State-11	$D_3, S_2, D_1, S_7, S_D, S_4, S_5$	16V _{dc}	$V_1 + V_2 + V_{C2} + V_3$	246.4
State-12	D ₃ , S ₂ , S _B , S _A , D ₁ , S ₇ , S _D , S ₄ , S ₅	15V _{dc}	$V_2 + V_{C2} + V_3$	231
State-13	D ₃ , S ₂ , S _A , S ₇ , D ₂ , S ₄ , S ₅	$14V_{dc}$	V1+Vc1+V2+V3	215.6
State-14	$D_3, S_2, D_1, S_7, D_2, S_4, S_5$	$13V_{dc}$	$V_1 + V_2 + V_3$	200.2
State-15	D ₃ , S ₂ , S _B , S _A , D ₁ , S ₇ , D ₂ , S ₄ , S ₅	$12V_{dc}$	V ₂ +V ₃	184.8
State-16	$D_3, S_2, S_4, S_7, S_8, S_5$	11V _{dc}	$V_1 + V_{C1} + V_3$	169.4
State-17	$D_3, S_2, D_1, S_7, S_8, S_5$	10V _{dc}	V1+V3	154
State-18	D_3, S_2, S_3, S_4, S_5	9V _{dc}	V ₃	138.6
State-19	SA, S7, SD, S4, S1, S2	8V.4c	$V_1 + V_{C1} + V_2 + V_{C2}$	123.2
State-20	$D_1, S_7, S_D, S_4, S_1, S_2$	7V _{dc}	V1+V2+VC2	107.8
State-21	SD, S4, S5, S6, S7	6V _d	$V_2 + V_{C2}$	92.4
State-22	S _A , S ₇ , D ₂ , S ₄ , S ₁ , S ₂	5V _{dc}	$V_1 + V_{C1} + V_2$	77
State-23	$D_1, S_7, D_2, S_4, S_1, S_2$	4V _d	V1+V2	61.6
State-24	D ₂ , S ₄ , S ₅ , S ₆ , S ₇	3V _{de}	V2	46.2
State-25	S ₄ , S ₇ , S ₈ , S ₁ , S ₂	2V _{dr}	V ₁ +V _{C1}	30.8
State-26	D_1, S_7, S_8, S_1, S_2	V _{dc}	V ₁	15.4
State-27	S ₁ , S ₂ , S ₂ , S ₄	0	0	0
State-28	D1, S6, S5, S4, S3	-V _{dc}	-V1	-15.4
State-29	SA, S6, S5, S4, S3	-2V _{dc}	- (V1+VC1)	-30.8
State-30	D_2, S_3, S_2, S_1, S_8	-3V _{de}	-(V ₂)	-46.2
State-31	$D_2, S_3, D_1, S_6, S_5, S_8$	-4V _{dc}	$-(V_1+V_2)$	-61.6
State-32	$D_2, S_3, S_4, S_6, S_5, S_8$	-5V _{dc}	$-(V_1+V_{C1}+V_2)$	-77
State-33	Sp, S4, S5, S6, S7	-6V _{dc}	$-(V_2+V_{C2})$	-92.4
State-34	$S_D, S_3, D_1, S_6, S_5, S_8$	-7V _{dc}	$-(V_1+V_2+V_{C2})$	-107.8
State-35	S _D , S ₃ , S _A , S ₆ , S ₅ , S ₈	-8V _{dc}	$-(V_1+V_{C1}+V_2+V_{C2})$	-123.2
State-36	S_3, S_1, S_8, S_7, S_6	-9Vdc	-V ₃	-138.6
State-37	$D_1, S_6, D_3, S_1, S_4, S_3$	-10Vdc	-(V1+V3)	-154
State-38	S _A , S ₆ , D ₃ , S ₁ , S ₄ , S ₃	11V _{dc}	$-(V_1+V_{C1}+V_3)$	-169.4
State-39	D ₂ , S ₃ , S _B , S _A , D ₁ , S ₆ , D ₃ , S ₁ , S ₈	$12V_{dc}$	-(V ₂ +V ₃)	-184.8
State-40	D_2 , S_3 , D_1 , S_6 , D_3 , S_1 , S_8	13V _{dc}	$-(V_1+V_2+V_3)$	- 200.2
State-41	D_2 , S_3 , S_A , S_6 , D_3 , S_1 , S_8	$14V_{dc}$	$-(V_1+V_{C1}+V_2+V_3)$	-215.6
State-42	S _D , S ₃ , S _B , S _A , D ₁ , S ₆ , D ₃ , S ₁ , S ₈	15V _{dc}	$-(V_2+V_{C2}+V_3)$	-231
State-43	S _D , S ₃ , D ₁ , S ₆ , D ₃ , S ₁ , S ₈	16V _{dc}	$-(V_1+V_2+V_{C2}+V_3)$	-246.4
State-44	S _D , S ₃ , S _A , S ₆ , D ₃ , S ₁ , S ₈	17V _{dc}	$-(V_1+V_{C1}+V_2+V_{C2}+V_3)$	-261.8
State-45	S_E, S_1, S_8, S_7, S_6	$18V_{dc}$	-(V ₃ + V _{C3})	-277.2
State-46	$D_1, S_6, S_E, S_1, S_4, S_3$	$19V_{dc}$	-(V ₁ +V ₃ +V _{C3})	-292.6
State-47	$S_A, S_6, S_E, S_1, S_4, S_3$	$20V_{dc}$	$-(V_1+V_{C1}+V_3+V_{C3})$	- 308
State-48	D2, S3, SB, SA, D1, S6, SE, S1, S8	$21V_{dc}$	-(V ₂ +V ₃ + V _{C3})	-323.4
State-49	D ₂ , S ₃ , D ₁ , S ₆ , S _E , S ₁ , S ₈	$22V_{dc}$	$-(V_1+V_2+V_3+V_{C3})$	-338.8
State-50	D ₂ , S ₃ , S _A , S ₆ , S _E , S ₁ , S ₈	$23V_{dc}$	$-(V_1+V_{C1}+V_2+V_3+V_{C3})$	-354.2
State-51	S _D , S ₃ , S _B , S _A , D ₁ , S ₆ , S _E , S ₁ , S ₈	$24V_{dc}$	$-(V_2+V_{C2}+V_3+V_{C3})$	-369.6
State-52	S _D , S ₃ , D ₁ , S ₆ , S _E , S ₁ , S ₈	$25V_{dc}$	$-(V_1+V_2+V_{C2}+V_3+V_{C3})$	-385
State-53	S _D , S ₃ , S _A , S ₆ , S _E , S ₁ , S ₈	26V _{dc}	$-(V_1+V_{C1}+V_2+V_{C2}+V_3+V_{C3})$	-400.4

Table I Consistently generating voltage in accordance with 53 MLI Conduction Switches

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7)PD-PWM for 53 level-MLI

Both basic switching (low switching frequency) and PWM modulation control schemes are used in the Modulation Control Scheme. The PWM Phase Disposition Technique with a 20 kHz switching frequency is utilised in this ACHMLI. PD-PWM is employed to control the inverter's switches.

IV.SIMULATION RESULTS a) EXISTING RESULTS 17 LEVEL MULTILEVEL INVERTER



Fig 5. MATLAB/SIMULINK circuit diagram of 17-level Multilevel Inverter



Fig 6. Simulation (a) o/p voltage and (b) waveforms of current of (17-Level Multilevel Inverter

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Fig.7 THD of output voltage

33 LEVEL MULTILEVEL INVERTER



Fig .8 MATLAB/SIMULINK circuit diagram of 33-level Multilevel Inverter



Fig.9. Simulation (a) o/p voltage and (b) waveforms of current of 33-Level Multilevel Inverter

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Fig.10 THD of output voltage

53 LEVEL MULTILEVEL INVERTER WITH P&O MPPT TECHNQUIE

A 215W solar panel has been designed, with the relevant parameters and specifications listed in TABLE 2. TABLE 2. Specifications of the 215W PV system

Maximum power	213.15W
The voltage at maximum power point (V _{MPP})	29V
Open circuit voltage (Voc)	36.3V
Current at maximum power point (I _{MPP})	7.35A
Short circuit current (Isc)	7.84A
Diode ideality factor	0.98117
Diode saturation current (Io)	2.9259×10 ⁻¹⁰ A



Fig 11. MATLAB/SIMULINK circuit diagram of overall structure of the 53 level MLI system with P&O MPPT.



Fig 13. waveforms of the 53-Level MLI (a)out voltage and (b)current

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Fig.14. THD% of Voltage

b)EXTENSION RESULTS

PROPOSED THREE PHASE 53 LEVEL MULTILEVEL INVERTER WITH IMPROVED INC MPPT TECHNQUIE

TABLE-3 solar PV parameters

Maximum power	240W
Vmpp	32V
Voc	38V
Impp	7.55
Isc	7.89





Fig 15. MATLAB/SIMULINK circuit diagram of overall structure of the 53 level MLI system for EV with proposed improved incremental conductance MPPT.



Fig.16 Subsystem of three phases 53 level-MLI

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Fig.17 53 level-MLI for one phase



Fig.18 Boost converter simulation waveforms. (a) Vboost (b)Iboost



Fig .19 Three-phase (a)output voltage and (b)output current



Fig.20 Speed of the motor

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FIGURE 21. THD% of Voltage

THD COMPARISION TABLE

	EXISTING (P&O MPPT TECHNQUIE)	EXTENSION (IMPROVED INCREMENTAL CONDUCTNACE MPPT)
THD OF VOLTAGE	1.75%	1.58%

CONCLUSION

The suggested solar PV connected three phase 53-level Multilevel inverter topology for Electric Vehicles is implemented and executed to reduce the size and cost of the inverter, thus enhancing reliability and efficiency. An enhanced incremental conductance method based on the MPPT methodology has been used to assure a constant output. Compared to P&O MPPT, INC provides a faster response time. Use PD PWM for controlling multilevel inverter. For applications utilizing renewable energy, this topology is ideal.

FUTURE SCOPE

Renewable energy applications can benefit from the proposed multilevel inverter. Intelligent algorithms can be used to optimize the switching angle in a closed loop control. Future scope of the suggested work places more emphasis on the hardware implementation.

REFERENCES

- [1] J. Rodriguez et.al., "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [2] L. Tranquillo et.al., "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [3] K. K. Gupta et.al., "A novel multilevel inverter based on switched DC sources," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3269–3278, Jul. 2014.
- [4] L. Zhang et.al., "A family of five-level dual buck full-bridge inverters for grid-tied applications," IEEE Trans. Power Electron., vol. 31, no. 10, pp. 7029–7042, Oct. 2016.
- [5] R. Agrawal et.al., "Comparison of reduced part count multilevel inverters (RPC-MLIs) for integration to the grid," Int. J. Electra. Power Energy Syst., vol. 84, pp. 214–224, Jan. 2017.
- [6] K. K. Gupta et.al., "Multilevel inverter topologies with reduced device count: A review," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 135–151, Jan. 2016.
- [7] C. Dhananjay et.al., "Design and implementation of multilevel inverters for fuel cell energy conversion system," IEEE Access, vol. 8, pp. 183690–183707, 2020.

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- [8] Y. Suresh et.al., "Investigation on hybrid cascaded multilevel inverter with reduced DC sources," Renew. Sustain. Energy Rev., vol. 26, pp. 49–59, Oct. 2013.
- [9] Z. Li, P. Wang et.al., "A novel single-phase five-level inverter with coupled inductors," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2716–2725, Jun. 2012.
- [10] J. Ebrahimi et.al., "A new multilevel converter topology with reduced number of power electronic components," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.
- [11] J. Salmon et.al., "Single-phase multilevel PWM inverter topologies using coupled inductors," IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1259–1266, May 2009.
- [12] M. S. W. Chan et.al., "A new switched-capacitor boost multilevel inverter using partial charging," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 12, pp. 1145–1149, Dec. 2007.
- [13] B. Axelrod et.al., "A cascade boost-switched capacitor-converter-two level inverter with an optimized multilevel output waveform," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 12, pp. 2763–2770, Dec. 2005.
- [14] Y. Hinako et.al., "A switched-capacitor inverter using series/parallel conversion with inductive load," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878–887, Feb. 2012.
- [15] J.-M. Shen et.al., "Five-level inverter for renewable power generation system," IEEE Trans. Energy Convers., vol. 28, no. 2, pp. 257–266, Jun. 2013.
- [16] B. P. Divakar et.al., "Implementation of a voltage multiplier integrated HID ballast circuit with dimming control for automotive application," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2479–2492, Jul. 2009.
- [17] S.-J. Park et.al., "A new single-phase five-level PWM inverter employing a deadbeat control scheme," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 831–843, May 2003.
- [18] C. Dhananjay et.al., "Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads," IEEE Access, vol. 6, pp. 738–746, 2018.