ISSN: 0974-5823 Vol. 7 No. 6 June, 2022

*International Journal of Mechanical Engineering*

# SPEED CONTROL OF BLDC MOTOR USING MULTILEVEL INVERTERS AND PWM GENERATION USING ANN

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Abstract: The paper proposes the new concept with advance topology based three phase inverter with neural networks and FPGA. In this paper presents the usefulness of FPGA and neural networks in the power electronic converter applications. The FPGA is greatly used in high frequency power converters and in this paper the control of PWM pulses using FPGA and neural networks is proposed to run a motor in a rated speed. Firstly the three phase inverter is designed with only six power electronic switches and the output is connected to BLDC motor. In next steps the speed is measured and a feedback is given to Neural networks controller, in which the PWM pulses are controlled using FPGA to control the speed. Thirdly, the Multisim is used to simulate the circuit operation with Verilog codes to obtain the desired output. In this paper, the motor speed is made controlled and made to run at a rated speed with the ANN, which is difficult when we use the conventional techniques.

Keywords: FPGA, NN, Verilog, Multisim.

## I. Introduction

In the power electronic converter applications, the word “inverter” represents a class, with a conversion of dc voltage source to a ac current source. The use of single phase or three phase inverters has widespread applications in the world of power electronics. Now a day the Multi-level inverters also find the applications in power electronic industries. In industries the design **[5]** of inverters with high frequency is a new issue, hence the use of embedded and VLSI application will be the best solution to the problem. Since the FPGA is equipped with long development period and program re-usability feature, it is greatly considered in the industries **[15].**

The inverter output is an alternating current (ac) which is given to the load (Motor), the constant output voltage is also a new issue, to reduce voltage outages. The use of neural networks with Fuzzy logic and FPGA is the best solution for the problem.

**The figure 1 shows the block diagram of basic inverter, which takes DC voltage as input signal and gives out an AC signal as output.**

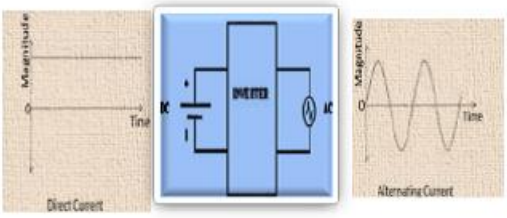


Fig 1: Block diagram of Inverter

The inverter gives AC voltage from DC voltage, here the output of an inverter will be a square wave form represents a two level inverter that is Vdc/2 and –Vdc/2.

This method is very effective and simple but it creates high distortion at output voltage. Hence the multi-level inverter concept came into existence to get the same output in different stated as stepped waveform instead of extracting output in two stages. Due to increase of voltage levels the waveform will be smooth and lesser THD value, but there will be an increase in complexity.

Multi-level inverter are of 4 types they are Diode clamped, Capacitor clamped inverters, Cascaded H-bridge inverter and Hybrid inverter.

Three level inverter:

Three level inverter produces three stages of output they are positive DC voltage, negative DC voltage and Zero voltage.

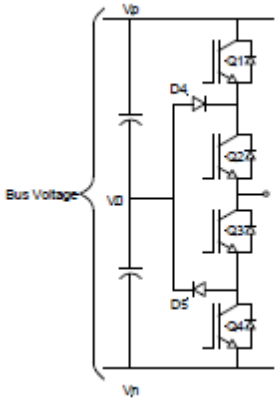


**Fig 2: Single phase three level inverter**

Figure 2 shows the three level inverter for single phase, it consists of 4 switches and a neutral point in the middle. The neutral point divides the voltage into positive and negative stages. When the switches Q1 and Q2 are ON the output of the inverter will be positive DC voltage Vdc and the switches Q3 and Q4 gives the negative DC voltage –Vdc, the switches Q2 and Q3 gives the zero output voltage. It is advantageous when compared to two level inverter, as switching losses will be less.

**Five level inverter:**

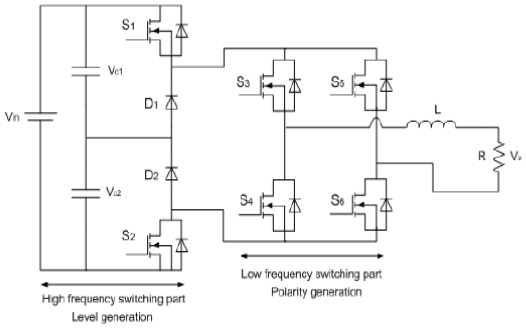


**Fig 3: Single phase five level inverter**

The figure 3 shows a single phase five level inverter. The output stages are Vdc, Vdc/2, 0, -Vdc/2, -Vdc.

1. The switches S1, S3 connects the positive end and Switches S2 and S6 connects the negative end to ground, remaining switches will be in OFF, this stage gives the Vdc output voltage.
2. Switches S1 and S3 connects positive end and Switches S4, diode D2 connects the negative end of the circuit, other switches will be OFF, the output of second stage is Vdc/2.

3. The zero voltage can be obtained without connecting to Vdc, switches S3 and S6, Diode D1 and D2 should be ON to get the Zero output voltage.
4. The switches S2 and S4 connect the positive end and Switches S1, S5 connects the negative end. The output of this stage is –Vdc.
5. The switches S2 and S4 are ON which connects the positive end and the switch S3 and diode D1 is ON, to get the output voltage –Vdc/2.

The high performance system is the key issue in the power electronic industries; therefore high performance power units should be designed with the creation of various different control techniques is very much needed to accomplish the specifications of the manufacturer.

The DSP processors are the first solution for the control techniques for several power supplies, but the DSP processors are not enough fast **[6]** for the real time applications and a small change in the program to introduction of new feature is long process, a huge revision of full program is needed. Hence the FPGA is a solution for program which is advantageous for real time application because of its long development period and software re-usability features. The FPGA **[7]** are also useful in high frequency circuits which is very much advantageous in the power electronic industries.

The code for FPGA should be in HDL (Hardware Description Language), either in VHDL/Verilog, comparatively the Verilog code is user friendly which is used in this paper. The problem associated with coding is with lengthy execution process apart from this the HDL code can be used efficiently for pulse generation.

The Artificial intelligence applications in power electronic control applications, including the electric motor drives has increased in last decade. The most common in artificial intelligence methods are Artificial Neural Networks- ANN and the Fuzzy Logic- FL, which are widely used in modeling and control applications [4].

The appearing growth in artificial intelligence, the neural networks are used for control of linear and non-linear loads, compared to other conventional techniques, ANN is more advantageous since it allows learning complex input-output mapping [5].

Hence the Artificial Neural networks are becoming more popular in the power electronic converter applications. The addition of feed forward in artificial neural networks is a key step in improving the dynamic performance. The neural networks collects the characteristic of the output, and artificially generates generated the training vectors and operate it for the desired output **[9].**

ANN is having the dynamic properties to improve the performance of the system. The control of power electronic converters in practice is efficiently accomplished by the ANN **[8]**. Artificial neural networks along with fuzzy logic are the emerging techniques which are present in ono-linear dynamical system, which van be used to improve the performance. In this paper Firstly the PWM pulses for three-phase inverter is generated with a Verilog code. Secondly, the pulses are simulated using FPGA module and thirdly these FPGA pulses are given to circuit to simulate using MATLAB Simulink and in the fourth step, the BLDC speed is controlled and made to run in a constant speed using ANN.

In the section II the basics of PWM technique is explained, the design procedure of generation of PWM pulses using FPGA is also given. In section III three the explanation of BLDC motor, its ratings and speed in rpm. In section IV the simulation circuit and the result waveforms and the Verilog output of PWM pulses for different Duty cycle is mentioned. In the section V the proposed system concluded with the future enhancement.

## II. PWM Techniques

In the PWM techniques basically it is divided into two methods i) Analog PWM technique and ii) Digital PWM technique. In Analog PWM technique, the carrier signal and a modulating is compared with the help of a comparator and the resulting waveform is itself a PWM signal **[8].**

The Analog techniques are further classified in 4 types, i) Sinusoidal Pulse Width Modulation. ii) Modified sinusoidal Pulse Width Modulation. iii) Single Pulse Width Modulation. iv) Multiple Pulse Width Modulation. The disadvantage of analog techniques is they are susceptible to noise and also they vary with temperature and voltage. [2,4], also there flexibility is less and they vary with a component variation [1].

Whereas the digital techniques are more flexible less prone to noise, fast processing, simple to design, many of the digital techniques will be constructed with a comparator based circuits.

Advantages of FPGA based design:

Field Programmable Gate Array is a best in designing of digital control scheme i.e. for PWM generation for power electronic converter applications. The design is simple, FPGA **[12]** are defined as a interconnection of logic blocks. The main feature of FPGA is they are designed in such a manner that they can be easily changed if there is any requirement or there is any adding of feature in the system needed in future. This feature is called as software re-usability, which has made impact on market [1].

Field programmable gate arrays are the logical blocks which are used as controllers, the field programmable gate arrays contains thousands are logical gates whereas PLD controllers contains hundreds of logical gates [8], these FPGA's are well known for the integrated logic design. The FPGA's are very popular for the high precision performance even at low frequency that is little MHz frequency and also best performance for higher frequency that is hundreds of MHz, The FPGA's are having special computational analysis which can be reconfigurable gives the best precise output for hardware designs. The figure 5 represents the design flow of Verilog programming to simulate the circuit using FPGA and the figure 3 represents the internal structure of FPGA IC in which the Verilog program is dumped to generate the required PWM pulses.

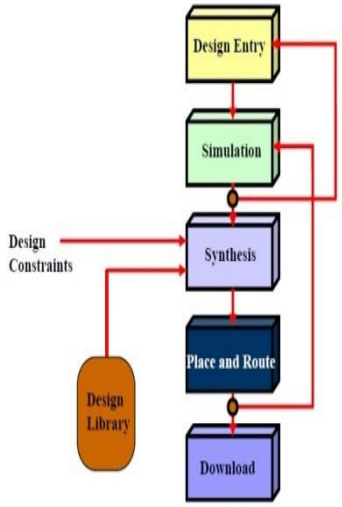


Fig 4: Programmable logic design process

Field Programmable Gate Array can be easily implemented in a short period of time, hence the FPGA is an efficient method to design PWM control technique. FPGA proves that it is also less costlier, hence they are economically suitable for small design. The PWM pulses generated using FPGA is by varying the duty cycle using Verilog code, in this paper the pulses are generated for two different duty cycles **[13].**

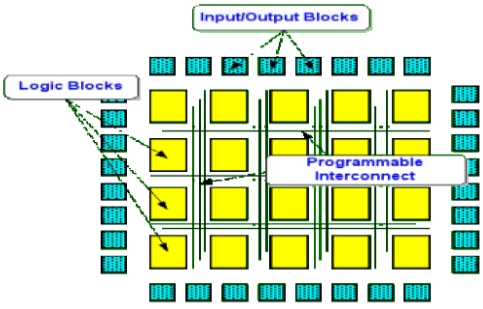


Fig 5: Internal structure of FPGA

The Artificial Neural Networks design consist of three basic types in which firstly the input layer is referred as input neuron, secondly the ANN has hidden layer referred as hidden neuron and thirdly the output layer

referred as output neuron. The input neuron function is to consider the input signals or reference signals to guide the hidden layer by the help of network point present in the input neuron; the output neuron generates the required output by considering the training process vectors represented by the hidden neurons. The figure 6 shows the ANN architecture with back propagation algorithm.

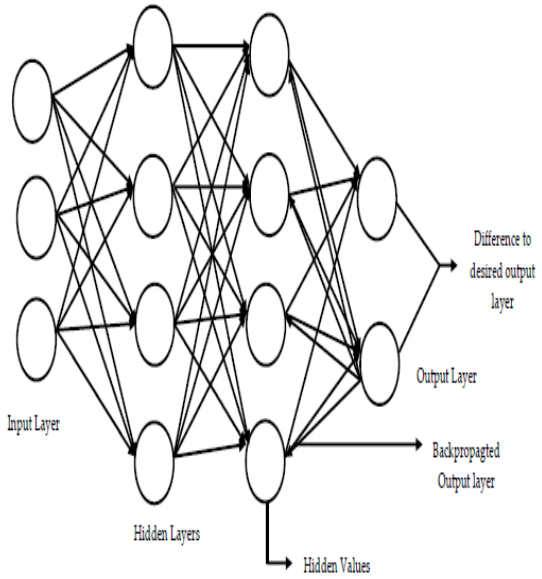


**Fig 6: ANN architecture (Back propagation algorithm).**

The output of the Artificial Neural Networks is to generate the constant voltage with the help of reference voltage to make the motor to run at a constant speed. The output of the controller is directed to the FPGA module.

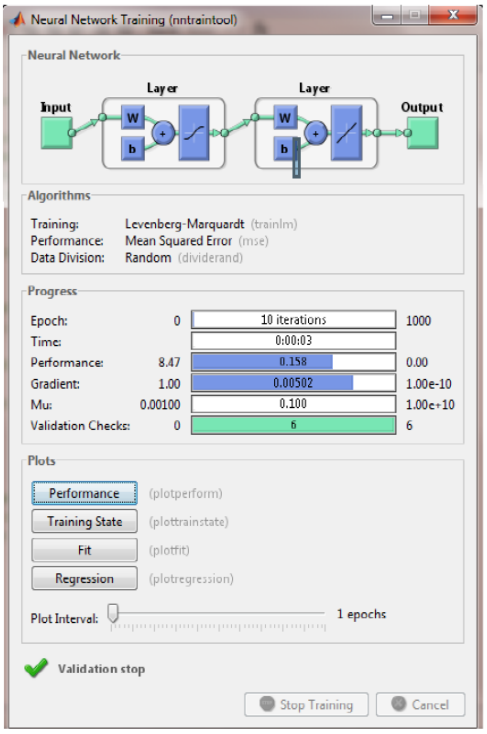


**Fig 7: ANN training process**

The figure 7 shows the simulation of ANN, in which the reference voltage is taken as the input layer and the output layer maintains a constant speed of BLDC motor with a constant voltage.

The Artificial Neural Networks are used to control the voltage, in this paper the controller is processed with ANN **[11]** and the output of the ANN is given to the FPGA, in which the duty cycle is varied with respect to the desired output i.e. the desired speed, The ANN controller receives the obtained speed, compares with the reference speed and then the error signal is generated and processed using the output characteristics incorporated in the controller, then the output of the controller is given to the FPGA module **[10],** where the code is executed according to the desired application, the PWM pulses so generated are given to the power electronic switches.

## III. About BLDC Motor

A word "Motor", is a device which converts a supplied electrical energy to mechanical energy. There are many types of motors in the market; here BLDC motors i.e. brushless DC motors are used by many industries because of its outstanding controllability, high efficiency and also a power saving features **[9].** Hence these features of BLDC motor gained the vast applications in power electronic industries.

The figure 6 shows the simple BLDC motor structure, the stator part in which two magnets of opposite poles are present, when the input is given, the magnets generate the magnetic field, the generated magnetic field and a electric current in a winding wire to induce force in the form of torque, which will be given to shaft of the motor.

The BLDC motors are more advantageous when compared to conventional motors, firstly it doesn't have commutator related problems. Secondly it is more efficient due to the use of permanent magnet rotor. Thirdly even in loaded and unloaded conditions the speed of operation is high due the absence of brushes which limits the speed. Low noise of operation since it is brushless. Electromagnetic interference is less and It has better dynamic response.

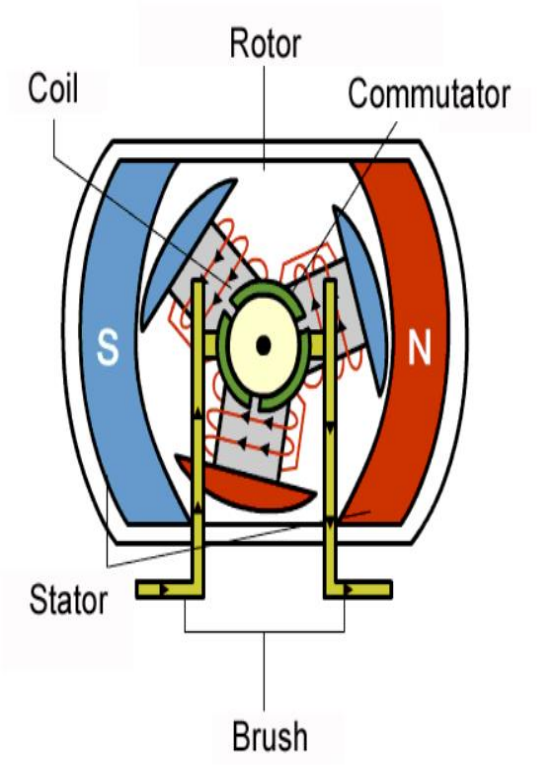


Fig 8: Brushless DC Motor

## IV. Simulation Circuit and Results

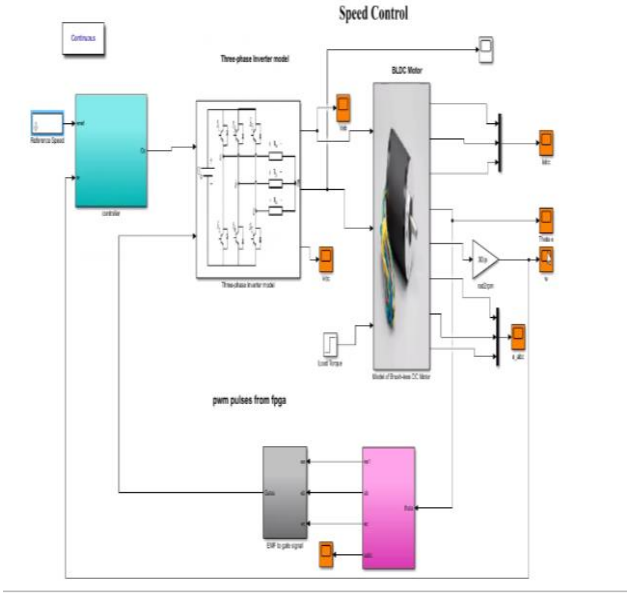


Fig 9: Simulation Circuit

The figure 9 shows the schematic of speed control of motor using ANN and FPGA. In this circuit firstly the reference speed is generated according to the industry demand, then accordingly the reference speed is given to the controller, the next part of the circuit is three phase inverter, which converts DC voltage to three phases AC used to run the BLDC motor **[14].** The output of the motor is measured in terms of voltage and also speed is measured and converted to radian value, which intern given to the controller that is the first part of the circuit, which is compared with reference speed and controlling action is carried using ANN and accordingly the FPGA pulses are generated to control on/off action of the switches to get constant reference speed as the output, which is obtained by varying the duty cycle. In the below figures the motor output, the inverter output and also the FPGA pulses with different duty cycle is given [10].

The figure 10 shows the inverter sine wave output of the three phase inverter and the figure 11 shows the BLDC motor output, which made to rotate with a constant speed using ANN.

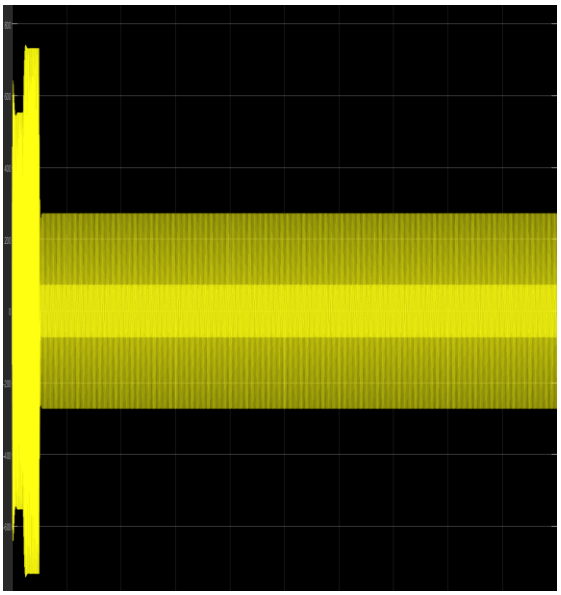

Fig 10: Inverter output

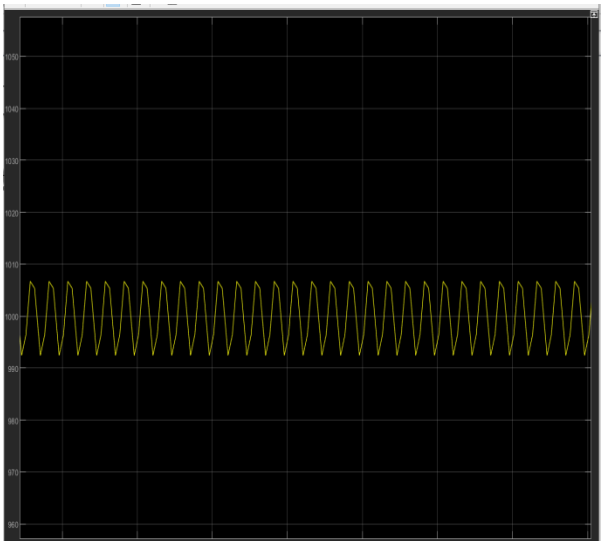

Fig 11: BLDC Motor output in rpm

RTL Schematic:

The below figures shows the RTL Schematic for different duty cycles, the Xilinx ISE simulator is used for pulses generation, the 4 bit output of the code is given to the ISE simulator from which the duty cycle is generated using the formula;

The equation 1 below represents the formula of generation of duty cycle in the Verilog programming, the integer value is the ON time period with respect to total time period.

$$Duty\ cycle = \frac{4\ bit\ word\ with\ a\ integer\ value}{16} \text{--------(1)}$$

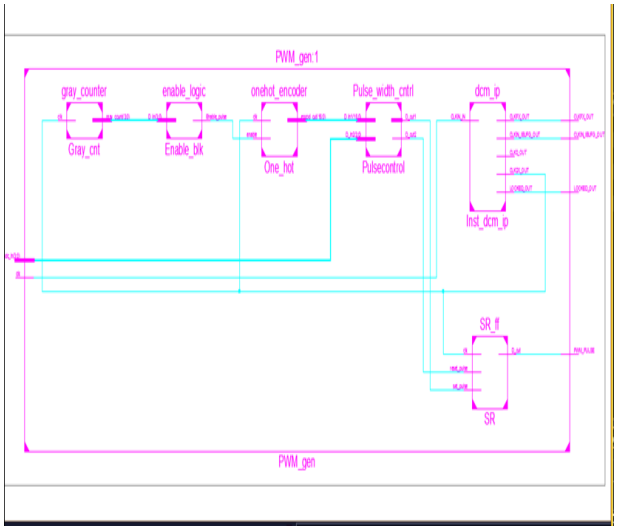


Fig 12: RTL schematic of proposed DPWM Architecture

The figure 12 shows the design synthesis of Xilinx, the Verilog programming is used to generate DPWM pulses by varying the duty cycle. The mathematical calculation of duty cycle is as shown in equation 1, the integer value is converted to a word (16 bit binary number).

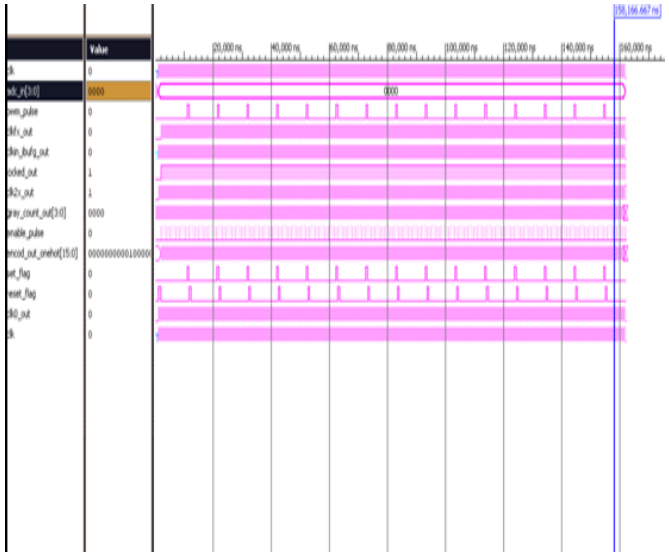

Fig 13: Behavioural Simulation for duty cycle =62.5%

The figure 13 and figure 14 shows the PWM pulses for two different duty cycle, here a analysis is made for generation of DPWM pulses with the Verilog programming with a FPGA hardware programmable device, so that the on and off time of switches in the inverter can be controlled digitally which makes more advantageous for real time applications, especially when there is application for high frequency operated switching devices [7].

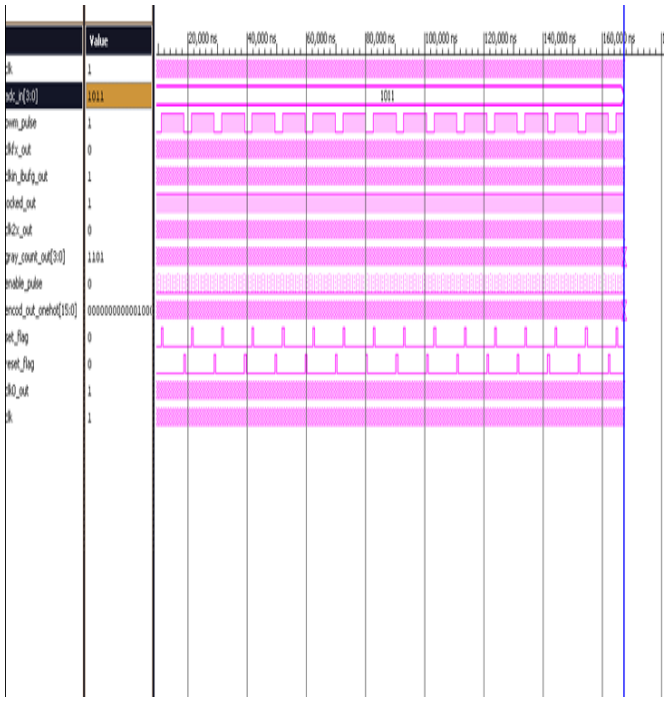

Fig 14: Behavioural Simulation wave for duty cycle 75%.

## V. Conclusion

In the proposed method the three phase inverter is designed with a constant speed BLDC motor with the help of ANN and also FPGA, the various PWM topologies are studied and generated the pulses with different duty cycle using Xilinx ISE. In this paper it is shown that the use of FPGA to control the inverter is the best way

when compared to conventional microcontroller or DSP technique, also in this paper the Motor is made to run at a rated speed using ANN and getting a smooth waveform as output. In future enhancement the same results are compared with the other intelligent controllers such as Fuzzy logic and Neuro-Fuzzy system.

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