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Design and Implementation of Adaptive Digital Filter Using Novel Carry Generation Adder & Multiplier

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ABSTRACT: In this paper design and implementation of adaptive digital filter using novel carry generation adder & multiplier is developed. Basically, digital filters are most widely used in the applications of high speed and DSP. Initially, input is given to First In First Out block (FIFO) and the FIFO will transfer the data to data memory block to save the memory. Cyclic Redundancy Check (CRC) will check whether the obtained data contains any errors. If there are any errors then CRC will detect and modify that data. Next arbitration logic is applied to the obtained data for high speed. The data will be passed to the adaptive filter block to perform addition and multiplication operations. All these data will be saved in the register bank. The adaptive digital filter is simulated using tanner tools technology. From results itcan observe that number of MOSFET's, nodes and delay are reduced in very effective way.

Key Words: Cyclic Redundancy Check (CRC), FIFO (First In First Out), MOSFET's, Nodes, Delays, Adder, Multiplier, DSP (Digital Signal Processing), Memory Bank, Data Memory, Arbitration Logic, CMOS (Complex Metal Oxide Semiconductor).

1. INTRODUCTION

There are many ways for designing of digital filters. Each filter design is suitable for particular application in time-domain or in frequency domain. Filters for the time-domain applications are specially designed to conserve the signal shape because the information is encoded in the signal by the source [1]. Therefore, filters in this domain are employed to preserve the shape of waveforms like signal restoration, suppressing of DC components and smoothing.

Unlike time-domain, the shape of the signal is not significant in frequency domain.

Because the signals in the frequency domain contain periodic waveforms, the phase, frequency and amplitude of the signals holds the information. Therefore, filters in this domain are employed to allow certain band of frequencies which holds necessary information. Signal separation is main objective of frequency domain filters.

Apart from the filters in two domains other filters are used known as custom filters. The functioning of custom filter is different from the remaining two. This type of custom filters designed to remove the unnecessary convolution that means to perform deconvolution [2]. These are three types of filter according to their use. It can classify filters in other way based on the filter structure exploited for realization of the filters

Conversion of that data faces challenges if CMOS implementations are used. Mainly there are two challenges. Most difficult and first challenge tedious thing is that integrating of ADC's with each and every channel or pixel since analog circuits have large area. This is highlighted by poor analog circuit scaling in CMOS because advanced technologies have various process variations [3]. Second one is that ADC's higher static power. To balance the performance and area/power, most of image sensors with high speed uses image sensor in sensor arrays in column parallel ADC's.

One of the widely used filter among different classes of digital filters is moving average filter. It is a widely used filter due to ease of implementation and the ability to suppress the random noise. Moving average filter is a superior filter among all time-domain filter, because it preserves the edges of step response during its filtering operation. The frequency domain characteristics of the moving average filter is contrast to the time-domain. This filter cannot separate frequencies appropriately. Some other filters like Gaussian, Blackman filters show improvement in response characteristics than moving average but, at a cost of high calculation time.

One of the convolution type techniques in the frequency domain is windowed-sinusoidal filter. The function of this kind of filters is to distinguish band frequencies from the other. It offers excellent stability in their frequency response characteristics. Efficient performance of the filter is not possible in both domains [4]. The desired frequency domain performance can be achieved at expense of loss of time-domain characteristics such as ripples in pass-band and overshoot. Windowed-sinc filters when implemented with standard convolution method are simpler to program but the execution is slow. The speed can be increased with fast Fourier transform.

In some unique applications general filters like low-pass or band-pass are not suitable for the specific task to be performed. A technique is described here for implementation of digital filters with irregular frequency response, customized to the requirements of specific application is custom filtering. Digital filters in DSP surpass analog filters with the ability to resolve conflicts while designing of custom filters. These filters are employed to perform two specific tasks such as deconvolution and optimal filtering. Deconvolution is used to

remove the effect of unnecessary convolution from the signals. Whereas optimal filtering is used to distinguish the frequency spectrum which was overlapped.

Generalized filters could not able to recover actual signal transmitted properly. Therefore, a special filter is required to remove the unwanted convolution. The main objective of that filter is to compensate for convolution by using deconvolution procedure [5]. In order to perform deconvolution, the convolution characteristics must be known. Otherwise it is called as blind deconvolution which is a complex problem in custom filtering. The problem of blind deconvolution cannot be resolved by usual methods, different approaches that customized for specific application are used.

It is not possible to identify convolution in time-domain, however much easier in frequency domain. This unwanted convolution modifies amplitude and phase of the actual transmitted signals. The main objective of the deconvolution procedure to restore the original signal by compensating these amplitude and phase transformations

2. TYPES OF FILTERS

There are four widespread filters present in the frequency domain. They are Low pass, high pass; band pass and band reject filters. The desired features of these four common filters are shown in the figure (1). The resultant frequency response of the low-pass filter is transformed to realize remaining four filter characteristics. In designing of filters Low-pass filter is highly focused because this can extract all other filter forms using low-pass frequency response. For transformation from low-pass to high-pass there are two well-established methods known as spectral inversion and spectral reversal.

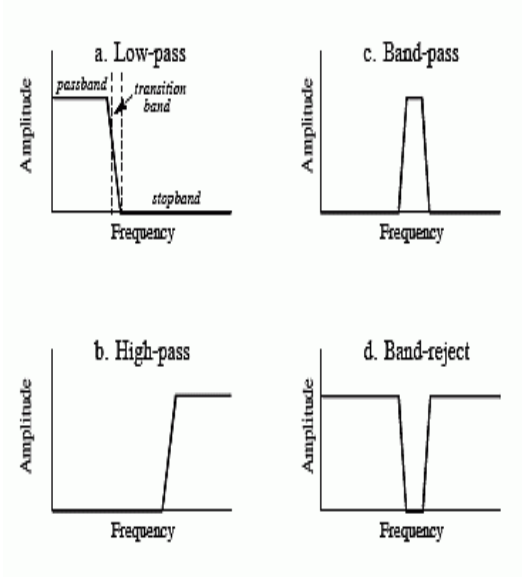

Fig. 1: FOUR COMMON FILTER FREQUENCY RESPONSES

Low pass and High pass filters: One of the filter conversion methods is spectral inversion is illustrated in figure 2(a). It is a low pass filter kernel. Although the filter kernel in the figure consists of 51 points as its length, lot of them has very less values which look like almost zero. The frequency response of the filter corresponding to low pass kernel is depicted in figure 2(b). The frequency response is obtained by performing FFT after padding 13 zeros (to make 64-point FFT) to the kernel.

The conversion to high-pass is a two-step process. First step is to inverse the sign of the each sample in the filter kernel. Second step of the process is to add the sample in the middle of the symmetrical kernel. The resultant filter kernel looks like as shown in fig 2(c) with corresponding frequency response in fig 2(d). The spectral inversion method turns over the frequency response from up-to-down. It converts low pass to high pass by transforming pass band to stop band and stop band to pass band. Similarly converts band-pass to band-reject.

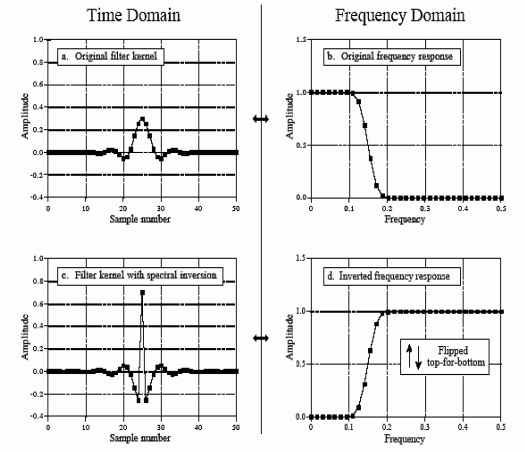

Fig: 2 a) LOW-PASS FILTER KERNEL b) FREQUENCY RESPONSE OF LOWPASS FILTER KERNELc) HIGHPASS FILTER KERNEL d) HIGHPASS FILTER FREQUENCY RESPONSE BY SPECTRAL INVERSION

High-pass filter realization from the inverted spectrum of low-pass filter can be achieved by using two methods illustrated in figure 2. The first method in 2 (a) consists of low-pass filter, which generates impulse response h (n) to input signal x(n). Another filter is an all-pass filter which produces impulse response delta function $\delta(n)$ for the given input x(n). The corresponding outputs from two filter stages are given to the adder circuit. In this the low-pass filter response gets deducted from all-pass filter response. So that the resultant will be high-pass filter output denoted by y(n). The above process can easily be implemented using computer program without need of additional hardware. In this program the low-pass filtered signal is subtracted from the actual signal. The total operation is performed in a single step by adding two filter kernels together.

The band pass and band reject filter are also implemented using filter responses of most common low pass and high pass filters. The band-pass filter frequency response is obtained by cascading of two filters. The convolution is performed between frequency responses of low pass filter and high pass filter. The band-reject filter frequency response is obtained by addition of two filters. Spectral inversion of the band reject filter response produces the band-pass filter response. Several techniques like cascading, parallel structures of filters are used to implement several other filters.

3. ADAPTIVE DIGITAL FILTER USING NOVEL CARRY GENERATION ADDER & MULTIPLIER

The below figure (3) shows the block diagram of adaptive digital filter using novel carry generation adder & multiplier. Initially, input is given to First In First Out block (FIFO) and the FIFO will transfer the data to data memory block to save the memory. Cyclic Redundancy check (CRC) will check whether the obtained data contains any errors. If there are any errors then CRC will detect and modify that data. Next arbitration logic is applied to the obtained data for high speed. The data will be passed to the adaptive filter block to perform addition and multiplication operations. All these data will be saved in the register bank.

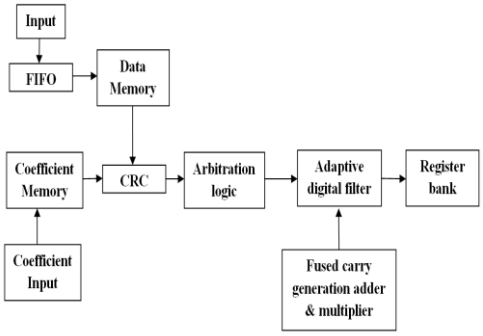

Fig. 3: BLOCK DIAGRAM OF ADAPTIVE DIGITAL FILTER USING NOVEL CARRY GENERATION ADDER & MULTIPLIER

The below figure (4) shows the schematic of adaptive digital filter using novel carry generation adder and multiplier. 280 MOSFET's are utilized while designing the circuit. Basically total nodes are classified into two types they are independent nodes and boundary nodes. 156 total nodes are utilized, 138 independent nodes and 18 boundary nodes are utilized while designing the circuit.

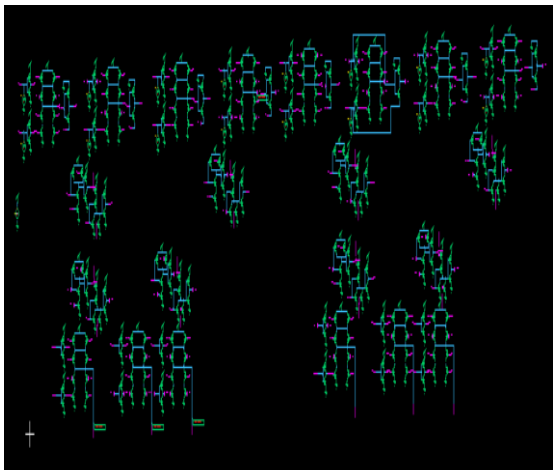

Fig. 4: SCHEMATIC OF ADAPTIVE DIGITAL FILTER USING NOVEL CARRY GENERATION ADDER & MULTIPLIER

The below figure (5) shows the input waveform of adaptive digital filter using novel carry generation adder and multiplier. Here, the A0, A1, A2, A3 and B0, B1, B2, B3 are the two four bit input information. Then the unfiltered outputs are p0, S1, S2, and S3. The A0=1, A1=1, A2=0, A3=1 and B0 =0, B1=0, B2=1, B3=1 are the given inputs and p0=1, S1=1, S2=1, S3=0 are the unfiltered outputs.

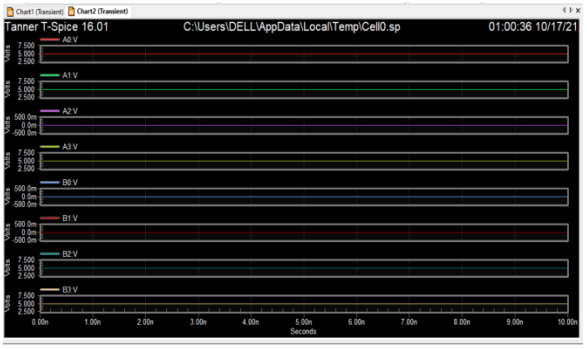

Fig. 5: INPUT WAVEFORM

The below figure (6) shows the Unfiltered outputs for given input.

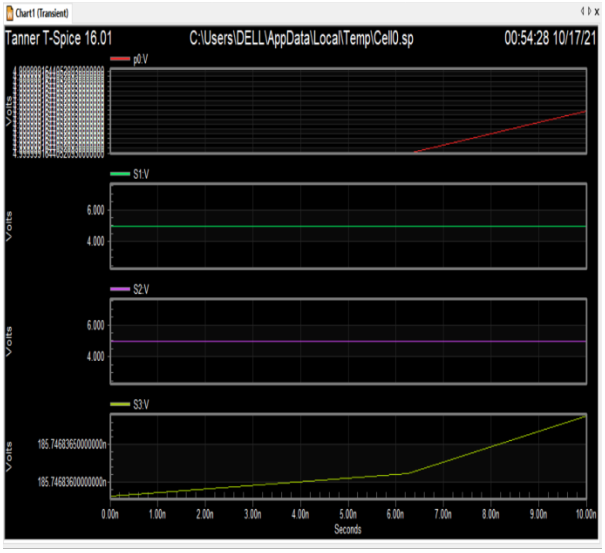

Fig. 6: UNFILTERED OUTPUT

The below figure (7) shows the filtered outputs for given input.The filtered output are considered as pp0, SS1, SS2, SS3 and are obtained as pp0=1, SS1=1, SS2=0, SS3=1.

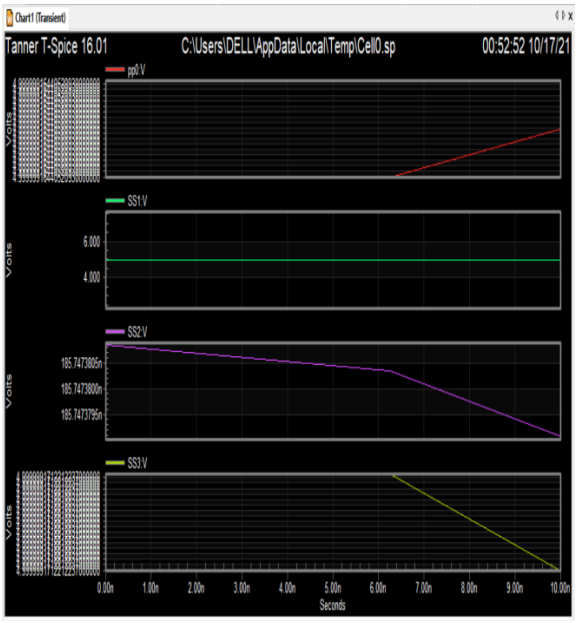

FIG. 7: FILTERED OUTPUT

The below figure (8) shows the delay representation of adaptive digital filter using novel carry generation adder and multiplier. In this delays are classified as total delay, overhead delay, parsing delay and set up delay.

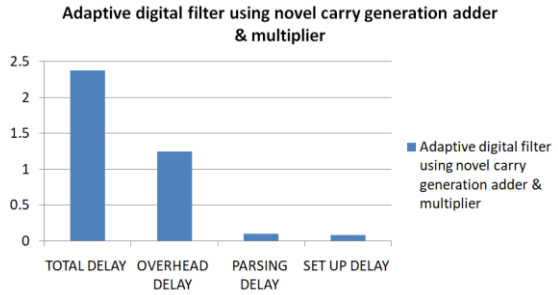

Fig. 8: DELAY REPRESENTATION

4. CONCLUSION

Hence, in this paper adaptive digital filter using novel carry generation adder & multiplier was implemented successfully. Adaptive digital filter using novel carry generation adder & multiplier will improve the speed of operation in very high way. From results it can observe that delay is reduced and nodes utilization is also reduced in very effective way. Usage of MOSFET's while designing this circuit is also very less which can observe from results.

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