ISSN: 0974-5823 Vol. 6 No. 3 December, 2021

International Journal of Mechanical Engineering

EFFICIENT FEEDBACK ENABLED RESTORABLE 10T STATIC RANDOM ACCESS MEMORIES USING FINFET TECHNOLOGY FOR LOW POWER APPLICATIONS

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ABSTRACT:

Memories play the key role in semiconductor industries as the informations to be stored are in plenty and hence the designing of these memories have become crucial as it requires reliable and power efficient design techniques. This research work aims at desiging a low leakage Static Random Access Memories (SRAM) which are much suitable for many low power applicational areas. To achieve this, two different methodologies are followed. The first one being the replacement of conventional CMOS technology to FINFET as the finfet transistors with their ability of double gate technology helps reduce sub-threshold leakage and leakages due to short channel effects. The second consideration focus on the design technique where the leakage reduction is achieved by adding source biased transistors on cross coupled inverter circuits. This source biasing helps in reducing the sub threshold leakage current. The proposed methodologies have achieved better 65% of power reduction and propagation delay has been reduced by 59%.

Key Words : Static Random Access Memories, SRAM, FINFET, Low leakage SRAM, FINFET SRAM

1. INTRODUCTION

Technology downscaling a crucial factor which has shaken the semiconductor world when headed towards least node values. Some of the high critical issues are leakages at sub-threshold level voltages, gate dielectric levels, major damages due to short channels and inter and intra device variations [1]. However the major challenging effort comes up when there is a drastic increase in the sub threshold leakge current [2]. These criticalities must be rectified by using a powerful and strong solution that not only minimise these effects but also improve the performance the device when compared to the previous CMOS technology nodes [3]. However, gate oxide thinning will help in reducing the reduction of both the gate leakage and in turn the gate-induced drain leakage (GIDL) [4]. This has enabled the researchers to identify the better option for overcoming these effects and ended up with the switching of a new device from the conventional CMOS devices [5]. The FIN shaped double gate transistors which are termed as FINFET transistors have bridged the gap that's created between the bulk CMOS and the need for technological growth [6].

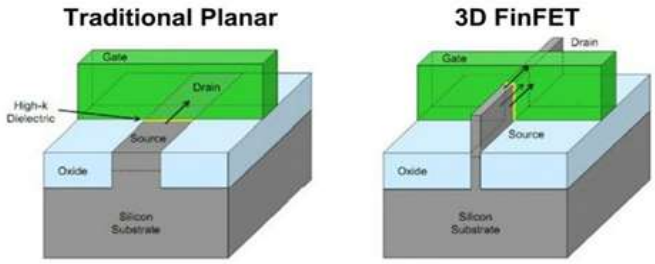

Figure 1: Planar structure of MOSFET and FINFET device structures

Figure 1 shows the planar structure for the device assembly for MOSFET and FINFET devices. Figure 1a shows the traditional two dimensional planar MOSFET transistor formation which has created a channel for current conduction during "ON" state in the region of silicon beneath the gate electrode. Similarly in the Figure 1b shows the three dimensional Tri-Gate formation of transistors which are conducting current using the channel formed on all the three sides which provides the operation of full depletion mode using the vertically arranged FIN structure [7]. Also from this we can understanf that FINFET structures has better control over the channel when compared to MOSFET. This will also help in reduce the effects of short channels when the channel length is reduced. By lowering short channel effects, switching speed can be improvised by merely reducing the static leakage of current in the channel and enhance the drive strength of the current. This helps in reducing the power consumption of the structure and hence can be much benefited than the conventional planar MOSFET structures.

There are basically two main classifications in FINFET which are Shorted Gate FINFET (SG-FINFET) and Independent Gate FINFET (IG – FINFET) as shown in Figure 2. SG FINFET structure will have only three terminals where both the front and back gate structures are shorted physically to form the same net and hence they can also be termed as Three terminal (3T) FINFETs. In case of IG FINFET, the structure will have four terminals where both the front and back gate teminals are left independent to each other to stand as independent terminals and hence they can also be termed as Four Terminal (4T) FINFETs [8].

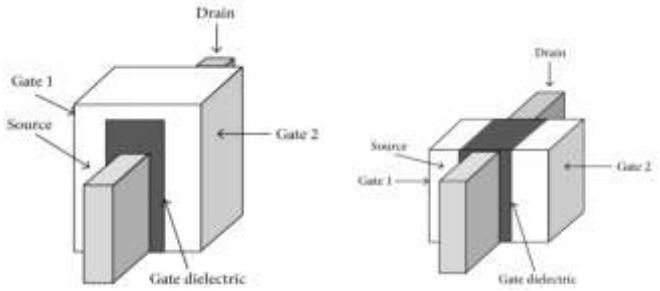

Figure 2: Structural view of SG and IG FINFET

Static Random Access Memories (SRAM) using the standard 6 transistors were the promising model used for many years as the Read and Write operation are very simple using lesser number of transistors. These memories almost consume 94% of the chip area in most of System-On-Chip(SoC) circuits [9]. Hence the performance of these memory circuits are very crucial when switching over to FINFET technologies. The foremost priortised propoerties to be considered in momory designing is their density, functionality and their performance[10]. The conventional 6T structure cannot be replicated in the FINFET structure and hence the designing and modelling of these memories are the key focus of this research work.

This paper is summarised as follows. Section 1 covers on the limitations on CMOS and the need for FINFET devices and an introduction on the structures and the basic introduction to SRAM memory. Section 2 covers the related works and researches which have been performed earlier in the SRAM design and FINFET structures. Section 3 covers on the transistor design methodology and the proposed SRAM circuits and its functionality on READ and Write operation using FINFET transistors. Section 4 covers the performance of the proposed circuit and thereby analysing the parametric factors like Power, delay and Power Delay Product (PDP). The final section covers the conclusion and future scope of this research work.

2. RELATED WORKS

Rajendran S., Mary Lourde R. (2020) [11] confirmed that the leakage current and power dissipation can be lowered by using the quasi planar FINFET structures instead of the regular MOSFET-based memory and described the modelling methodologies and simulation methods of a double-gate n-FinFET structure. The optimization of 6T FinFET based SRAM cell can be implemented by modifying the width and pitch of the fin structures.

Shilpi Birla et.al (2020) [12] have analyzed SRAM design using 8T FinFET for both Shorted Gate and Low powered Independent Gate mode where the later helps to improvise the stability and enhance the performance of the circuit and the results have been compared for 20nm technology model. The results shown good improvisation when using LP based IG mode than the SG mode operations.

David Burnett et.al (2014) [13] have discussed the design challenges of SRAM in FINFET technology. Due to the lower supply voltage, write operation is much more affected than the read operation hence a write assist technique is needed for the write operation. They also provided the tradeoff information between the cell size and Vmin for the FINFET configurations for various nodes.

Rajeev Ratna vallabhuni et.al (2020) [14] implemented 6T SRAM structure in both the conventional MOSFET and 18nm FINFET technology node and examined the performance of both the structures by analyzing various parameters like power, leakage using the FINFET spectre models.

Deepika Sharma & Shilpi Birla (2021) [15] proposed two different SRAM design using FINFET technologies. Both the design structure are designed using 10T which analyze Static and dynamic power consumption, Static Noise Margins (SNM) for Write, Read and Hold. Static Noise Margins, Static and dynamic power consumption. The proposed cells have different read path and write path and the design have been analysed for both the power and stability using Independent Gate (IG) FINFET. The proposed IG FINFET obtain highest margin value and lowest power consumption.

3. METHODOLOGY

This section covers on the FINFET characterisation and proposed SRAM design strutcutres using the FINFET transistors.

3.1 FINFET Transistor Characteristics

Continuous change in feature size and its resultant modification in the photolithographic limitation will drastically cause statistical fluctuations in electrical device parameters like threshold voltage (Vt), On Current (I_{on}) and Off-Current (I_{off}). This will cause device mismatch and hence affect the performance of the circuit and in turn affect the yield of the die. This is the major impact factor that's limiting the scaling of MOSFET.

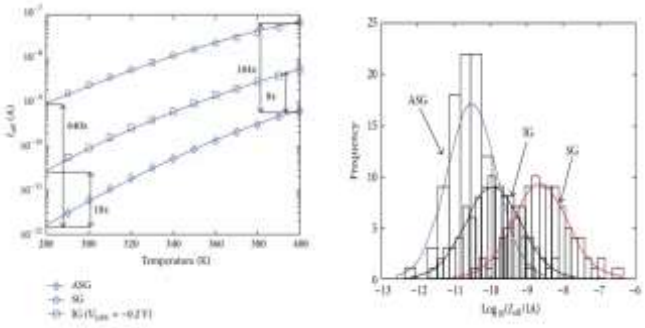

Figure 3: I_{off} distribution under process variation for various FINFETs

Like MOSFET structures, FinFETs will also encounter process variations. As the dimensions of the FINFETs are small and due to the limitations in lithographic methodologies, FINFETs too are exposed to various fluctuations mainly in the thickness in both fin and gate-oxide and gate length and so on [16]. From figure 3, it is clearly understood that temperature variation has severe impact in FINFET structures as the oxide layer below the fin structures exhibit lesser thermal conductivity. Hence the Ioff distribution under process variations have also been analyzed and SG and IG FINFETS have good performance in terms of process variations.

3.2 SRAM Design structures

SRAM is the important and basic building block in the state-of-the-art microprocessor units. In recent years, it is confirmed that more than half of the die area will be occupied by SRAM.

Hence memory density is another crucial parameter to be considered while designing the memory core chip. Another crucial parameter to be considered is the leakage power which SRAM exhibit as they have extensive idle periods in the bulkiest memory arrays. Below figure 4 shows the 6T FINFET SRAM which have been the conventional model of reducing the leakage power and variability.

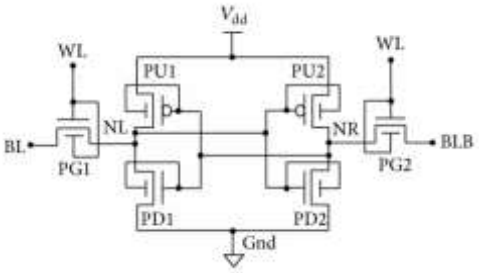

Figure 4: Conventional Six Transistor FINFET SRAM structure

During Write operation, additional write assist circuitary will be added that provides data information to Bit-Line (BL) and Bit-Line Bar (BLB) which are complementary signals. These signals helps in storing information to the memory location. During Read operation, based on the Word Line (WL), Pull Up and Pull down transistors (PU1,PU2,PD1,PD2) helps in reading out the information through the Pass Gate (PG) transistors PG1, PG2 to BL and BLB signals through NL and NR nodes.

The proposed 10T SRAM structure as shown in the below figure 5 has 2 cross coupled inverters having on left and right side. The left side inverter consists of Pull Up transistor 1 (PU1), Pull Intermediate 1 (PI1) and Pull Down 1 (PD1) and right side inverters are formed using the Pull Up transistor 2 (PU2), Pull Intermediate transistor 2 (PI2) and Pull Down transistor 2 (PD2).

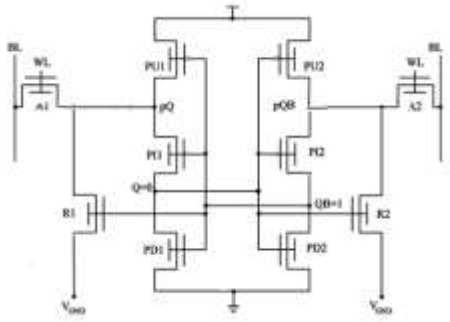

Figure 5: Proposed 10 Transistor FINFET SRAM structure

These combination of PFIN-PFIN-NFIN structure will generate the feedback loop path. This will be much helpful during read operation to restore the informational nodes and also will be useful during standby mode of operations. The restoring path will be formed with the help of transistor pairs A1 and PI1 for the data to Q signal and A2 and PI2 for the data to QB signal.

3.2.1 Memory Write operation

During Write operation, the signals BL and BLB are prechaged to VDD and GND respectively. To perform Write operration, Word Line (WL) has to be enabled which in turn enable the active transistors A1 and A2. PU1 and PD1 plays the crucial role in storing information bit to the Q signal and similarly PU2 and PD2 plays the vital role in writing bit value to the QB signal. The role of PI1 and PI2 is to limit the write operation by enabling the separation path to storage points and the isolated path.

3.2.2 Memory Read Operation

During Read operation, the initial criteria to be followed is pre-charging of Bitlines BL and BLB. Second step is to enable the Word Line (WL), then the access transistors (A1, A2) and then R1 will be turned on to read out data from Q and R2 will be turned on to read data fromm QB. But both R1 and R2 are not turned on simulataneously. The reading happens based on the voltage variation between the Bitlines BL and BLB which helps to read out the data from the Q or QB storage nodes. The read stability is improved by the intermediate transistors PI1 and PI2 which provides the feedback path that helps to restore the data information.

4. RESULTS AND DISCUSSION

The Memory structures discussed in section 3 have been designed and simulated using the Syopsys HSPICE simulator using the 32nm FINFET PTM model files [18] and the waveform has been obtained using the Avanwaves tool. The conventional 6T SRAM circuit has been implemented using FINFET technology for both Write and Read operation and the simulated waveforms are analysed for the functionality and the performance measures are analysed using parameters like power, delay and power delay product (PDP).

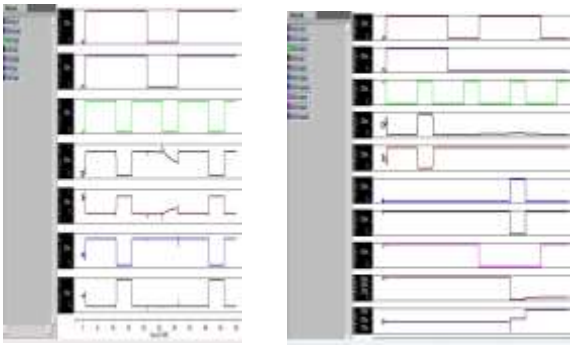

Figure 6: Simulated waveform for write and read operation using 6T SRAM FINFET

The Write operation of simulated waveform using 6T SRAM is shown in Figure 6 a where when the WL and Wen(Write Enable) is high, data input din is replicated in q and qb output through bitlines bl and blb. Similarly read operation simulated waveform using 6T SRAM is shown in Figure 6 b which shows when the WL is high and Wen is low (Which performs read operation), data in the q signal is read out at out siganl whenever sensing of the signal happens.

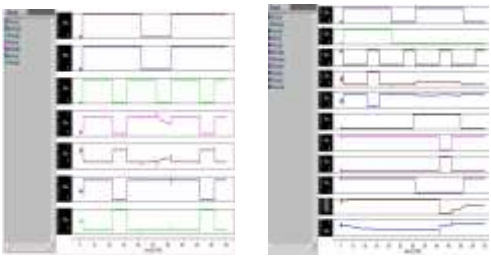

Figure 7: Simulated waveform for Write and Read operation using 10T SRAM FINFET

The Write operation of simulated waveform using 10T SRAM is shown in Figure 7 a which is similar to the conventional write operation but witht the difference on the PPN inverter path where when the WL and Wen(Write Enable) is high, data input din is replicated in q and qb output through bitlines bl and blb. Similarly read operation simulated waveform using 10T SRAM is shown in Figure 7 b which shows when the WL is high and Wen is low (Which performs read operation), data in the q signal is restored using the feedback path and the data is read out at out siganl whenever sensing of the signal happens with the help of the intermediate transistors.

Table 1 : Performance Evaluation for FINFET SRAM Design Structures

S.No.	Circuit	Power(µw)	Delay(ns)	PDP(FJ)
1	6T SRAM FINFET Write	9.812	4.899	48.82
2	6T SRAM FINFET Read	32.934	18.122	596.76
3.	10T SRAM FINFET Write	19.024	2.01	38.40
4.	10T SRAM FINFET Read	38.14	15.223	580.96

The performance analaysis is carried out for Power, Delay and PDP which has been analysed have been tabulated in the Table 1 where for the Write operation 10T SRAM consumes higher power than regular 6T but the delay has been reduuced which makes the PDP to be the most prominent factor to analyse the performance of the circuit and the lesser the PDP the performance is improvised.

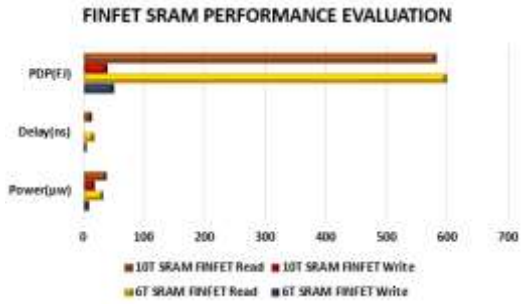

Figure 8 : Performance Evalaution chart for FINFET SRAM

From this inference from performance analysis chart as shown in figure 8, it is clearly seen that the the proposed 10T circuits exhibit lesser PDP when compared to the conventional 6T SRAM and hence the proposed structure can be used for further designing of the memory circuits.

5. CONCLUSION

Memory design structure enhancement has been the key focus on this research work, where the conventional CMOS circuit has been replaced with the Tri-gated FINFET structure. Using the Independent Gated FINFET structure 6T SRAM and 10T SRAM structures have been designed and analysed for parameters like power, delay and PDP. The sinulated results shows that power component shows a slight higher and the delay has been reduced. Hence PDP acts as the deciding parameter for the performance evaluation and the proposed 10T FINFET SRAM structure exhibits 22% of PDP reduction during Read operation and 26% of PDP reduction during Write operation. The future work of this research aims at further power reduction in FINFET SRAM designs and various other design structures will be performed t=for higher memory arrays.

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