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Study and Implementation of Band Gap Reference Circuit for constant Voltage Generation Using Foundry Based Mos Models

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Abstract

This study deals with the design of BGR Circuit. Also, detailed analysis of Foundry based MOSFET/BJT models will be done and shown in this work to give an insight on their characteristics. The BGR Circuit will con-sist of a current reference and generation Circuit, a PTAT and CTAT components which basically are Resistor and diode connected BJT respectively. This work will show the generation of Voltage which is PVT invariant and constant and corresponds to Bandgap of Semi-conductor device which intrinsic property of the same.

In the design of analog integrated circuit, it's important to create reference voltage and current with well-defined values. Bandgap reference are regularly used to achieve it on-chip. Especially in analog to digital conversion where the input voltage is compared to the several reference levels in order to determine the corresponding digital value, best application is this bandgap reference voltages. The main intention in this project is to understand the performance limitation as well as the design of band gap reference circuit, BGR. To study the circuit and implementation the tool used is CADENCE for schematic simulation and all of these circuits are implemented in 45nm cmos technology. Simulation have been done on Cadence tools for a temperature range of 45ºC to 125ºC are presented, showing that the new circuit is capable of working properly with either 1V and 1.2V supply voltages. Further characterization will be performed after the fabrication of the circuit.

Keywords→ BGR circuit, CTAT, PTAT, CMOS Process, MOS models.

1. Introduction

Bandgap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits [7]. Bandgap reference (BGR) circuits are widely used in modern LSIs to generate a

reference voltage on chips [6]. It produces a fixed (constant) voltage regardless of power supply variations, temperature changes, or circuit loading from a device. It commonly has an output voltage around 1.25 V (close to the theoretical 1.22 eV (0.195 aJ) band gap of silicon at 0 K) [8]. Reference voltage Generators are used in DRAM's, Flash Memories, and analog devices. This generator is necessary to stabilize the over process, voltage, and temperature variations [1] by Shigeru Atsumi. In the conventional implementation of Bandgap voltage reference generates an output voltage equal to 1.25V which is measured in electron volts. It cannot be used in latest deep submicron technologies. BGR circuits, was designed either be required an

external power on reset signal or to be composed of several MOS transistors for generating bias current, and the bandgap core circuit has two nodes that are controlled currents and voltages by resistors of the same value for generating the CTAT and PTAT currents [5]. Moore's Law only applies or is possible when the size of a transistor decreases exponentially over time. In 1965, Gordon Moore discovered that the number of transistors on a chip increased exponentially over time. When he predicted this, the size of the transistor was 100 µm [2] according to S. E. Thompson. There are many such circuit types in modern technology, the most popular of which is the bandgap reference voltage (BGR) because it can provide a predictable output voltage. [3] by E. Vilella. In this paper, we described about the transistor structure used in a 45nm generation CMOS logic technology compared with 180nm CMOS technology[3] designed for high speed and low power operation and all CMOS bandgap voltage reference circuit which is designed with a new startup circuit for self-biased opamp by using only one NMOS transistor and the bandgap core circuit is designed by defining the current and voltage with only one node and another node set equal voltage which can be controlled by input voltages of op-amp. A voltage reference is a simple block which remains constant against variation in operating voltage and temperature Fluctuations [4]. This method can reduce number of the resistor with a circuit solution suitable for low supply voltage operation and achieve the correct biased point at power on and successfully operate with near 1V supply voltage.

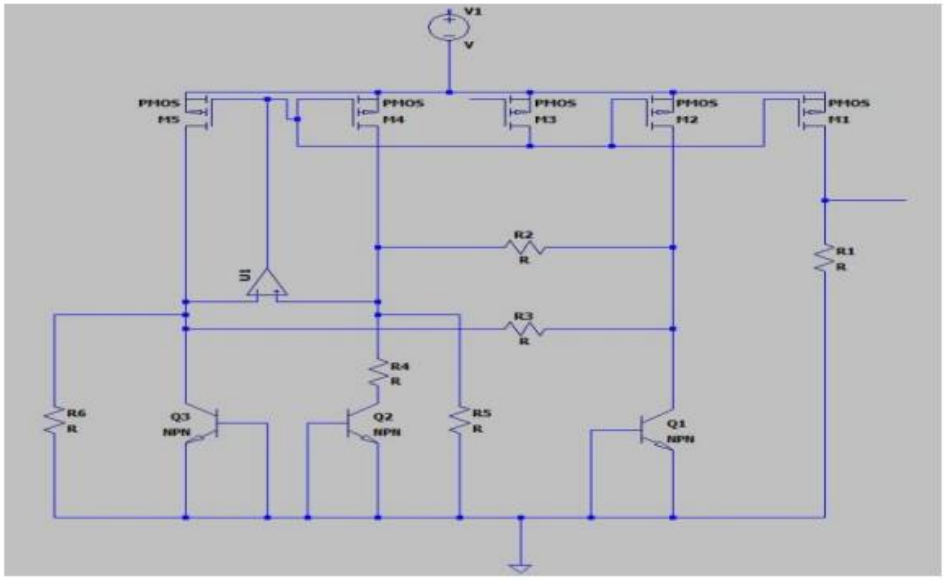

Figure1. Architecture of Curvature Corrected BGR

2. Need for Reference

The coordinated circuit ought to work at all temperature zones like desert and polar area. We want a reference voltage free of temperature so we can contrast it and another voltage that is reliant of temperature, and we can show how much is the genuine temperature. The reference should be independent of PVT variations:

P - Process: We have ICs manufactured on various processors, for example, CMOS 130nm, 65nm and so on.

V - Supply Voltage

T - Temperature: It should lie b/w - 40 to 125 degree Celsius.

We really want to distinguish CTAT and PTAT in the given circuit graph. We have (Vbe) as a CTAT voltage a positive terminal that will diminish w.r.t to temperature at a pace of - 2mV/c. The consistent current source (I1) is given. VT as Thermal voltage is a PTAT as at whatever point the temperature expands the voltage will likewise increments at a pace of +0.085mV/c. We have duplicate it with some number say M so the incline will increment to +2mV/c. After that we will get the temperature autonomous reference which is a consistent and aggregate it to come by the result BGR as:

$$Vout = Vbe + Mvt$$

2.2 CTAT Circuit

The voltage across a diode worked at steady current is corresponding to outright temperature (CTAT), with a temperature coefficient of roughly −2 mV/K. In the circuit, we have an ongoing source associated among Vdd and BJT which is a diode connector at whatever point authority and base are shorted and Vbe is Q1 which addresses the CTAT conduct.

2.3 PTAT Circuit

The voltage contrast between two p-n intersections (for example diodes), worked at various current densities, is utilized to create an ongoing that is relative to outright temperature (PTAT) in a resistor. This current is utilized to create a voltage in a subsequent resistor.

Table 1. Part values of the BGR and start up circuit

Parameter	Value@ Vdd= 1.3V	Unit
Temp Range	-40→125	℃
Vref@27℃	1.113	V
Max Δ Vref	49	mV
Power Consuption	213.1	μ

In the circuit, Presently guess we have 2 circuits with current source Ic in which first circuit has one semiconductor An and another circuit has n semiconductors nA.

→ Vbe = Vt ln (Ic/Is) (1)

The above equation is used to find the Vbe for both circuits. The first circuit with one transistor A will be written as:

→ Vbe1 = Vt ln (Ic/Is) (2)

The second circuit with n transistor nA will be written as:

→ Vbe2 = Vt ln (Ic/n / Is) (3)

Taking difference of (2) and (3) eqn. we will get PTAT quantity:

→ Vbe1 – Vbe2 = Vt ln(n) (4)

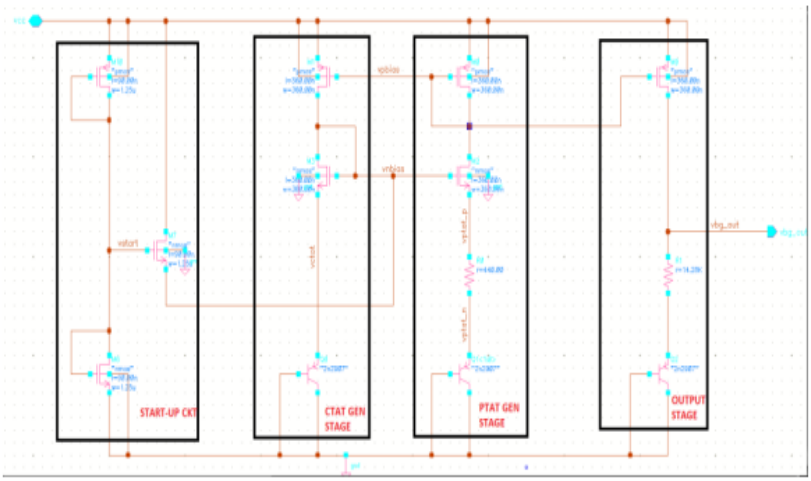

Figure 2. Combined CTAT and PTAT

3. Proposed BGR Circuit

We know that,

$$Vbe1 – Vbe2 = Vt \ln(n)$$

Here we have circuit utilizing an OP-AMP. We will compose Vbe1 at one semiconductor and due to virtual ground, anything that voltage will be at one terminal same voltage will goes on another terminal when the result gain is high. Subsequently, at positive terminal it is Vbe1. Presently voltage across R1 will be:

→ $VR1 = Vbe1 – Vbe2$

$= Vt \ln(n)$ (5)

Which is also called as PTAT voltage and Vbe2 is CTAT voltage.

Now,

→ $Vbgr = Vbe2 + Vt \ln(n)$ (6)

Ln(n) should be 23 so that we multiply it with CTAT to get +2mV/c

→ $Vbe2 + Vt (2)$ [11] (7)

Then,

→ $Vt \ln(n)/ R1 * R2$ (8)

So,

→ $Vbgr = Vbe2 + Vt \ln (n)$

$+ Vt \ln(n)/ R1 * R2$ (9)

→ $Vbgr = Vbe2 + Vt \ln (n)$

$[1 + R2/R1]$ (10)

→ $Vbgr = VCTAT$ (11)

Finally, we can understand that,

→ $Vbgr = Vbe1$

$+ Vt \ln (n) R2/R1$ (12)

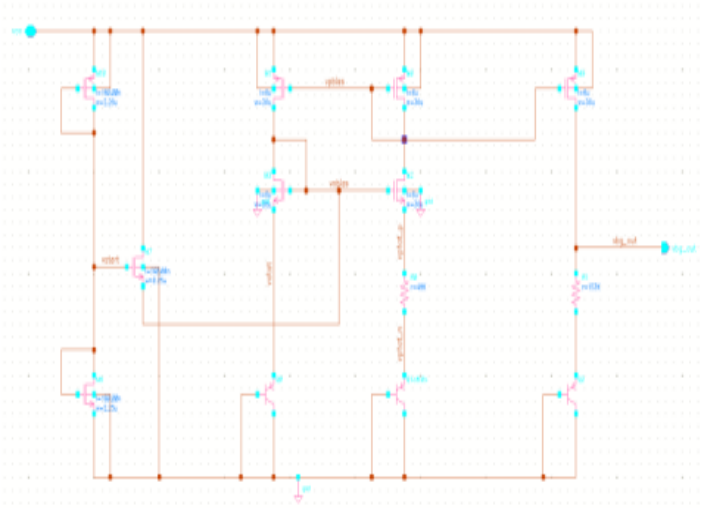

Figure 3. Proposed BGR Circuit 45nm

Table 2. Electrical Characterstics of the Proposed Circuit

Instances	Design Parameters
M10,M6,M7	W/L=1.25u/0.09u
M0,M1,M2,M3,M9	W/L=18u/0.36u
R0	0.44K
R1	14.28K
m	2

And Generated Waveform

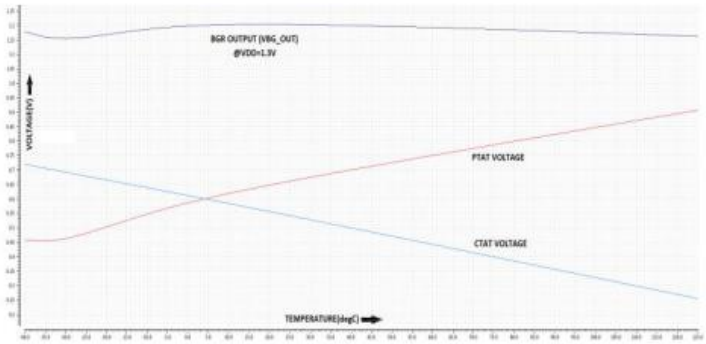

Figure 4. Waveform Generated

4. Conclusion

The plan or design of another radiation-lenient temperature remunerated BGR circuit in a standard 45nm CMOS innovation is proposed on tool CADENCE. To bear controlling at 1.2V, the managing framework considering resistors that empowers various voltage activity modes inside a similar circuit presented by this plan. Radiation resilience is accomplished using encased nMOS semiconductors and gatekeeper rings. Postformat reproductions for a temperature scope of -45ºC to 125ºC are introduced, showing that the new circuit is fit for working appropriately with either 1V or 1.2V stock voltages. Further portrayal will be performed after the creation of the circuit.

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