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Fractional order voltage balancing controllers for Grid side and Motor side MMC based variable induction motor Drive

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Abstract: MMC-based variable induction motor (IM) controller with fractional order voltage balance control is the primary objective of this research. A conventional modular multilevel converter (MMC) can't work at low frequencies because it lacks the requisite components for variable-speed induction motors. The SM capacitor's voltage fluctuates as the motor's rated torque decreases. It's not conceivable to end up with a system that runs on a zero-frequency motor. There have lately been proposals for an induction motor drive that does not require additional circulating current. The grid-side MMC produces a constant dc current output rather than a dc voltage source in this back-to-back configuration. This current source is used as an input by the motor-side MMC when driving a three-phase induction motor. SM capacitor low-frequency voltage ripple is shown to be constant due to the SM capacitor's dc current source being constant. When using average capacitor voltage control, individual SMs are not guaranteed to operate in a balanced manner. Fractional Order PID (FOPID) controller is required for back-to-back MMCs with individual SM capacitors, as this page details. Lastly, the proposed fractional order balancing controller is shown to operate the drive across a large speed range.

Key Words: Modular Multilevel Converter (MMC), Sub-Module (SM), Fractional Order PID (FOPID) controller, Induction Motor (IM)

I.INTRODUCTION

The modular multilevel converter can be a great asset in situations when a transformer is not necessary (MMC). MVVSDs benefit greatly from MMC's modularity and scalability as well as the superior waveforms and low average switching frequency it provides. Low-frequency voltage ripple is a common problem with conventional MMC submodule capacitors (SM). Motor supply frequency drops enhance the voltage ripple in SM capacitors between the highest and lowest voltage points [4]. This problem prevents the MMC from being utilised with variable speed drives. Between the ages of 5 and 14, it was discussed. More than three times the typical value of peak arm currents can be achieved by using extra common-mode voltage and circulating current-based techniques as described in [5]–[14]. The converter can be protected from overloading by using two MMCs side-by-side. An idc constant direct current is generated in line with the grid-side MMC in Figure 1. The motor-side MMC generates variable ac voltage and frequency. Even at extremely low frequencies, the voltage ripple of the SM capacitor remained constant. In MMC, either arm's SMs could be defective. Achieving an average capacitor voltage balance is difficult if the SM capacitor voltages in each arm aren't exactly the same. Distinct gate drivers have different features, semiconductor devices switch in unique ways, gate drivers age, and so on. Gate drivers are a good example of this. This can be caused by a variety of circumstances. As shown in [5]– [10] and [20], individual SM capacitor voltage is not regulated by the average voltage controller(s). Controlling both the average capacitance voltage and the individual capacitance levels necessitates two controllers. The output voltages and currents of the induction motor drive are distorted by utilising SM capacitors with varying voltages. These are called SM capacitors. Stability issues with the MMC converter might cause system trips. For best performance, an MMC-based induction motor drive must be correctly balanced. SM capacitor voltages in MMC-based drives have only been somewhat balanced. To keep the voltage of each SM capacitor constant, [1] presented a sorting strategy. [10–19] provides an additional repetition of this procedure. Unbalanced switching frequencies can increase converter losses when sorting algorithms are used. With many SMs in an HVdc application, sorting algorithms are typically used [19]. [2] and [20] SM capacitors can be balanced using pulse width modulation (PWM). (PWM). PWM control is utilised instead of a sorting method in MMC drives with a few tiny motors (SM). When there are fewer SMs, the sorting technique performs worse. PWM control enables high switching frequencies [20]. Both a common reference dc capacitor voltage and the balance controllers of individual SMs are used in the preferred motor-side MMC balancing method, according to [2] and [20]. The connection of these two controllers may have an effect on the convergence of the SM capacitor voltage in this case. All of these methods are appropriate for a regular MMC with a constant dc input voltage. Researchers have discovered that intelligent systems, variable structures, and fractional order derivatives/integrals can outperform conventional controllers in terms of performance and robustness. With a fractional-order PID controller, the dynamic features of the control system can be better regulated.

Capacitor voltage balancing using an MMC-based FOPID controller is discussed in this work. An intermediate constant dc current is used to manage the proposed control approach, which is specifically designed for back-to-back 9level-MMC setups as depicted

in Figure 1. From the drive's rated speed to its lowest potential speed, the suggested control algorithm must be tested to see how well it performs. As a result, the following is the structure of the article's content: To begin, the following paragraphs outline a grid-side MMC control mechanism. Motor-side MMC control strategy created by our team. Grid and motor MMC simulation waveforms, as well as proposed balance control procedures under various operating situations, are all included in the final report.

II.EXISTING SYSTEM

The grid-side MMC, seen in Figure 1, is set up for direct grid connection. It provides a regulated dc current source at the output while maintaining a sinusoidal grid current with a power factor of 1. The motor-side MMC drive takes its current from this source.

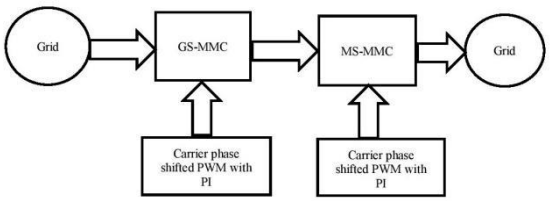


Fig.1. 1. Induction motor drive with three-phase back-to-back MMCs

III.PROPOSED SYSTEM

Back-to-back MMC indicator motors are depicted in Figure 2. An MMC is located on the motor side of the system, while the grid is on the motor side. To keep the voltages of individual SM capacitors constant, a fractional order balancing controller is proposed. Carrier phase shifting PWM is controlled by the GS-MMC and MS-MMC using a fractional-order PID controller.

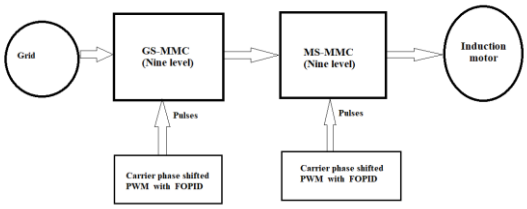


Fig 2 A back-to-back MMC-based indicator motor configuration has been proposed.

a) Modular Multi-level Converter (MMC)

MMC's standard sub-module (SM) layouts are shown in Figures 3 and 3. Each SM cell contains an IGBT switch T1, an anti-parallel diode D2, and a capacitor C.

The converter's phase leg is made up completely of SMs, which have two arms apiece. For the voltage difference between the upper and lower arms, an inductor is placed on each arm to compensate.

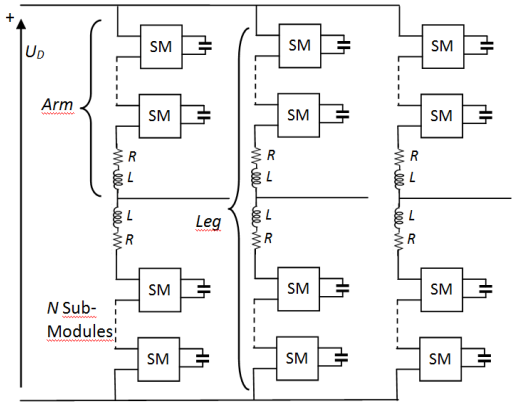


Figure 3 - Diagram of a three-phase Modular Multilevel Converter.

Using the SM in Figure 3, we can calculate the UO output voltage as follows:

UO = UC if *T1* is *ON* and *T2* is *OFF*

UO = 0 if *T1* is *OFF* and *T2* is *ON*

where UC denotes the voltage across the instantaneous capacitor.

As a result, turning on both T1 and T2 would result in a short circuit across the capacitor. When T1 and T2 are both off, the output voltage varies depending on the current direction. This arrangement is useless. Both useful current flows are shown in Fig. 3.8.

b) GS-MMC Controlling

Generation of Intermediate DC Current Source

To achieve balanced operation while using grid-side MMC, the legs of phases U, V, and W must generate equal quantities of direct current (dcg). The is created when the three leg currents work together to

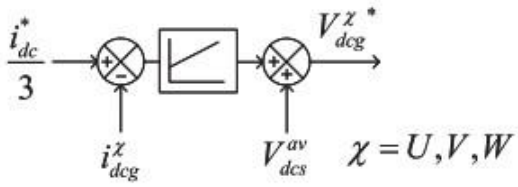


Fig. 4 Idc net dc current regulation at the intermediate level for all working conditions of the drive, idc is maintained at the same value.

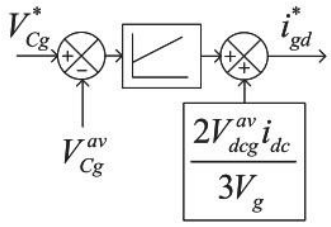


Fig. 5 The SM capacitor voltage is controlled by the grid-side MMC on an average basis.

The d-axis current command I gd is provided by the average capacitor voltage controller in order to meet the net active power requirement (Fig. 5). To keep each SM's capacitor voltage stable, this net active power must be distributed between the arms and SMs.

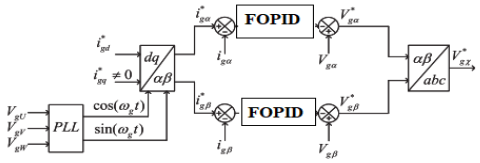


Fig. 6 Control of grid current.

Figure 4 depicts the relevant control block diagram. The q-axis current igq's magnitude is determined to compensate for the SMs' differences in power absorption. However, the SMs' absorption of active powers differs by a minuscule margin in practise. According to this article, the reactive current command should be set to 5% of the active current. I = GQ I = rated I = rated Gd

$$i_{gq}^{*} = 0.05 i_{gd}^{rated} \qquad (1)$$

The drive's rated input power factor is above 0.99.

Figure 6 shows SM capacitor voltage control options. This capacitor voltage controller has a smaller bandwidth than the inner grid current controller. Fig.7(a) shows a controller that ensures that the top and bottom V t Cgav arms of the grid-side MMC have the same average capacitance voltages. There are less voltage discrepancies in the arm with the individual SM balancing controller in Figure 7b.

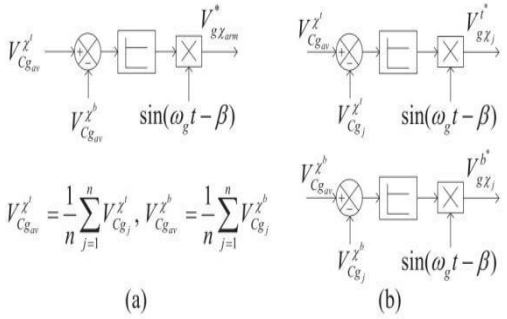


Fig. 7 Controllers for grid-side MMC capacitor voltage balancing.

Arm balancing controller (a). For each individual figure 5, 5, and 6 of the grid-side MMC, a single SM balancing controller (Figs. 8 and 9 respectively) is combined to deliver net voltage commands (V tg, V bg) for the top and bottom MMCs, respectively.

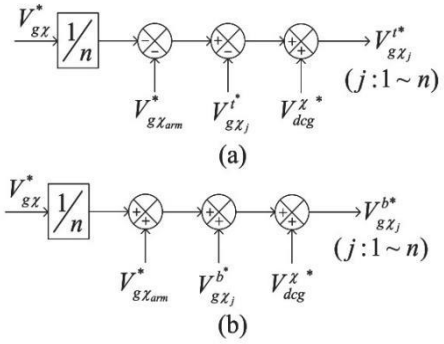


Fig. 8 Each SM of the grid-side MMC is given a voltage instruction. a The upper arm. (b) The lower arm

c)MS-MMC Controlling

Balanced Motor Currents Using Vector Control of Induction Motor

If the motor voltages are balanced, the three-phase windings of a three-phase induction motor produce balanced three-phase currents. Three-phase induction motors can be controlled with vector controllers (Fig. 9).

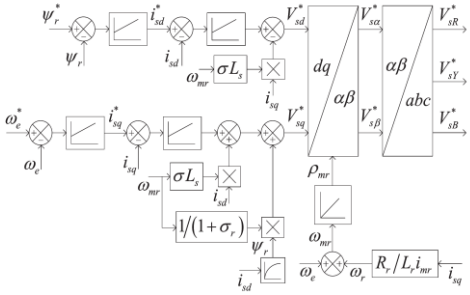


Fig.9 Induction motor drive rotor flux-oriented vector controller block diagram.

Average Capacitor Voltage Control and Distribution of DC Source Current

The motor-side MMC regulates the capacitance voltage of the SM capacitor by drawing active power from the idc source. V av Cs, the average capacitance voltage, is calculated dynamically by the motor-side MMCs for each SM.

$$P_s = \sum_{\lambda=R,Y,B} V_{s\lambda} i_{s\lambda} = 3V_s i_s \cos\varphi_s, V_{Cs}^{av}$$

$$= \frac{1}{6n}\sum_{\lambda=R,Y,B}\sum_{j=1}^{n}\left[V_{Csj}^{\lambda t} + V_{Csj}^{\lambda b}\right] \quad (2)$$

Vs and is are the rms values of the motor phase voltage and current. The power factor of a motor determines the input power (Ps) of the motor (s). The SM capacitance on the motor side is represented by Cs. SMs on the grid-side MMC have capacitance voltages V t Csj and V b Csj, respectively.

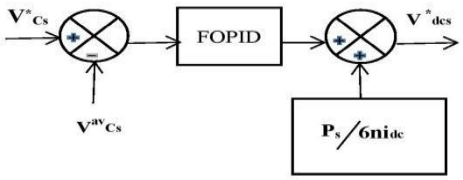


Fig. 10 Controlling the voltage of the SM capacitor on the motor side of the MMC using an average.

As depicted in Fig. 10, Vav Cs is managed by a FOPID controller in accordance with (5). Voltage command Vdcs is generated by this FOPID-controller. All SMs on the motor-side MMC receive the same amount of Vdcs.

With a gain Ks P proportional controller, the average capacitance of the top and bottom arms of the motor-side MMC is balanced, as shown in Figure 10. (a). An additional voltage reference for each SM is generated by this arm-balancing controller.

$$V_{Csarm}^{\lambda *} = K_P^s \left[V_{Csav}^{\lambda t} - V_{Csav}^{\lambda b}\right] \qquad (3)$$

Figure 11's overall average capacitance voltage controller is unaffected by average arm capacitor voltage controllers.

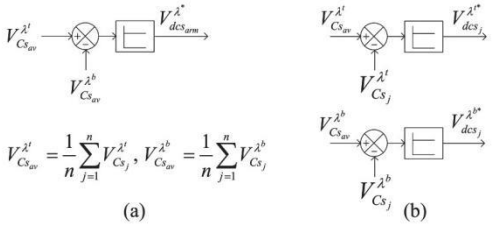
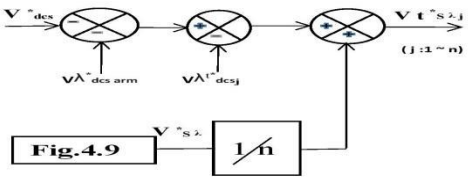


Fig. 11 CMMC controllers for motor-side voltage balancing. (a) Controller for arm balancing. (b) SM balancing controllers for each individual

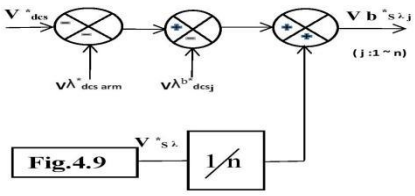
The difference between the average capacitance voltage of each arm and the individual capacitance voltage of each arm is applied to each arm to balance the capacitance voltage. The inaccuracy of each SM is multiplied by Ks P to get an additional DC voltage reference.

$$V_{Csj}^{b*} = K_P^s \left[V_{Csav}^{\lambda b} - V_{Csav}^{\lambda b}\right] \qquad (4)$$

This individual capacitor voltage controller has no effect on the average arm capacitor voltage controller.



(a)



(b)

Fig.12 Each SM on the motor side of the MMC receives a voltage command. (a) The upper arm. (b) The lower arm

FOPID CONTROLLER

A variation on the classic PID controller based on fractional calculus, the fractional order PID controller was invented by Podlubny in 1999. 5 offers the generic PID controller transfer function, where and need not be integers but can be any real number: P I D.

$$G(s) = K_P + K_I S^{-\alpha} + K_D S^{\beta} \qquad (5)$$

Developing a FOPID controller is more difficult than designing a typical PID controller because of the presence of five optimization parameters, KP, KI, KD, the use of optimization algorithms has led to several methods for this design being offered. This issue is not addressed in this work. In the simulation analysis of the system, iterations are used to determine the five parameters.

IV.SIMULATION RESULTS

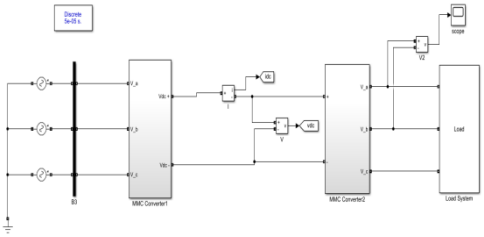


Fig.13 The suggested system's MATLAB/SIMULINK circuit.

A) EXISTING RESULTS (5 LEVEL MMC)

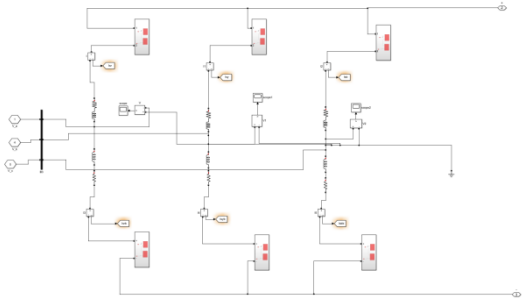


Fig .14 a five-tiered MMC

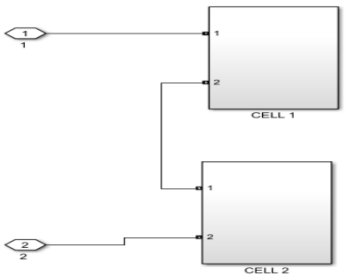


Fig.15 Positive arm of the five-level subsystem

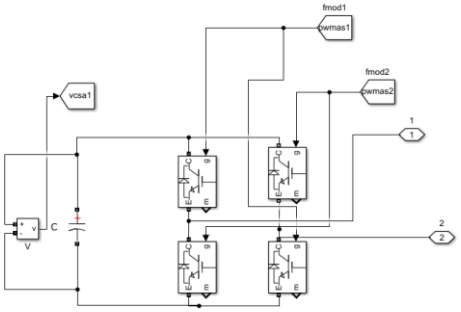


Fig.16 The cell's internal machinery

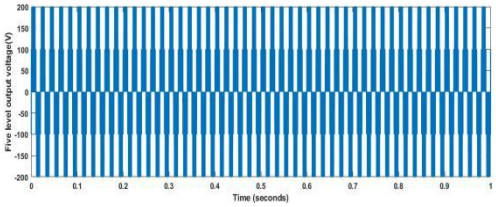


Fig.17 There are five levels of output voltage in this system.

CASE-1

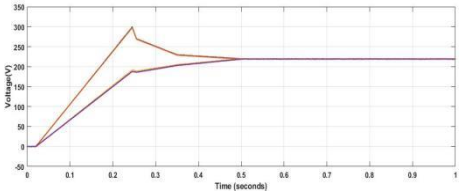


Fig.18 Without balancing control, the voltages of the SM capacitors of the grid-side MMC are not regulated.

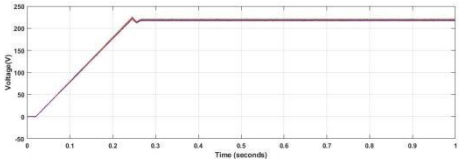


Fig.19 When the motor is not running: with the balancing control; grid-side MMC SM capacitor voltages

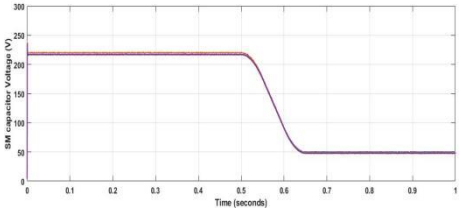


Fig .20 Voltages of SM capacitors on the grid-side MMC can rise rapidly when a sudden motor load is applied.

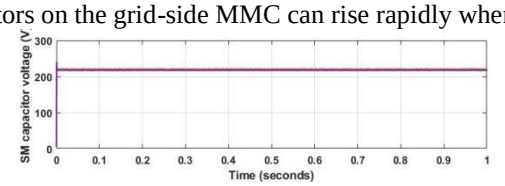


Fig.21 Balanced control voltages on SM capacitors of grid-side MMC are applied when the motor load suddenly increases.

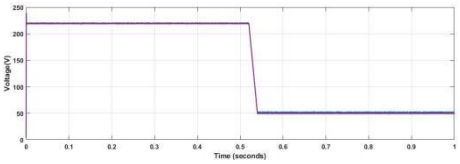


Fig.22 Balancing controls are deactivated if there is a high motor load. Capacitor voltages of one leg

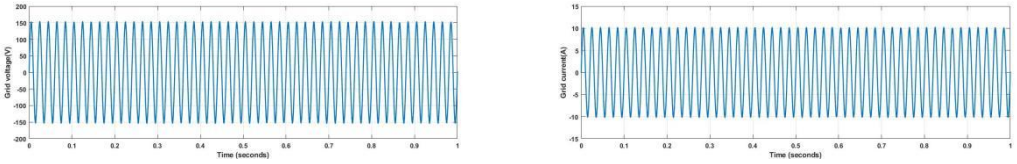


Fig.23 When the balancing control is turned off, the grid voltage and grid current are measured.

CASE-2:

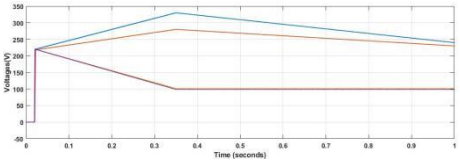


Fig.24 MMC voltages of the motor-side MMC when there is no load on the motor

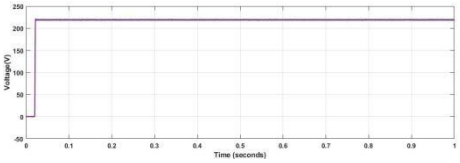


Fig.25 Balancing control with no motor load; SM capacitor voltages on the MMC side.

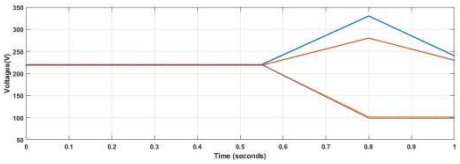


Fig.26 Voltages on the motor side MMC SM capacitor while balancing control is disabled.

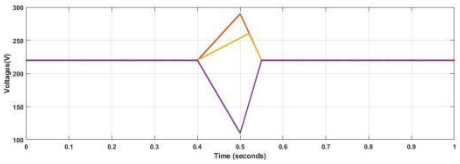


Fig.27 When the balancing control is turned off and then back on, the voltages on the motor-side MMC SM capacitors fluctuate.

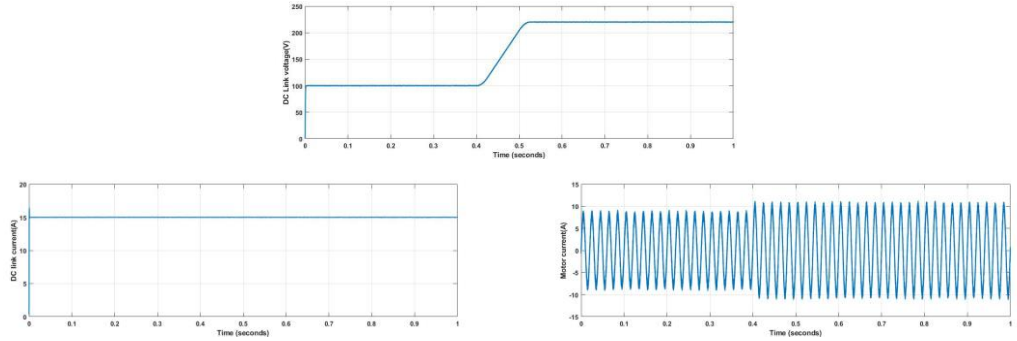
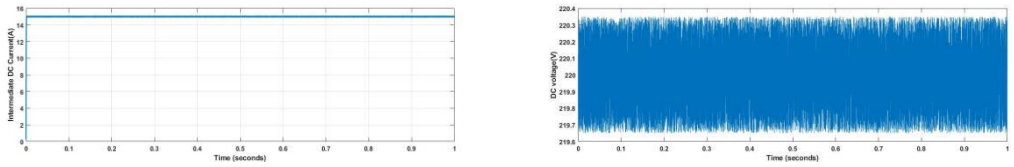
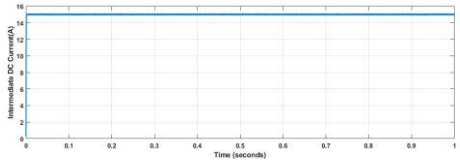


Fig.28 Motor current, dc-link current, and dc-link voltage command are all affected by abrupt motor loads.

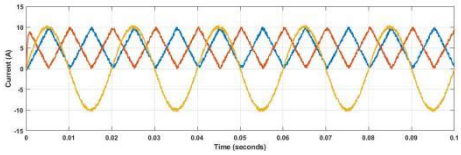
CASE-3



(a) Current and voltage in the intermediate dc range.

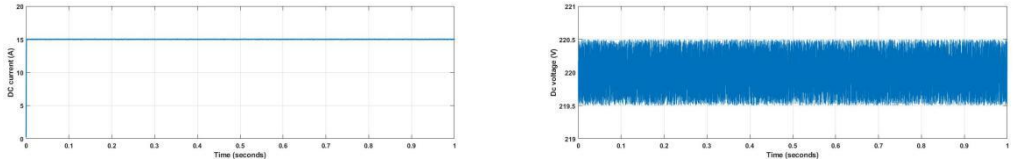


(b) Voltages across the SM capacitor on the motor side of the MMC.

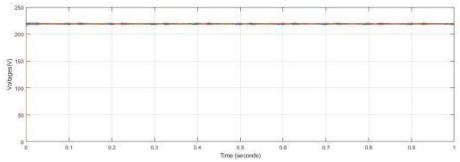


(c) Motor-side MMC currents in arms and motors.

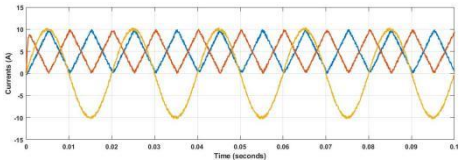
Fig.29 When s/2 = 51 Hz and rated torque is used, the simulated waveforms are shown.



(a) Dc current and voltage in the middle

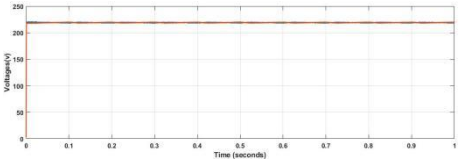


(b) Voltages across the SM capacitor on the motor side of the MMC.

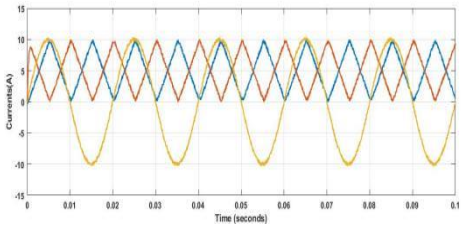


(c) Motor-side MMC currents in arms and motors.

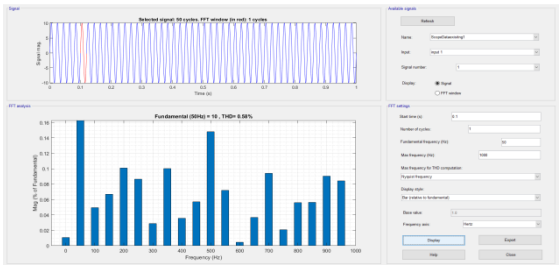
Graph 30 Simulation waveforms for s/2 = 27 Hz and rated torque are shown below.



(a) Voltages across the SM capacitor on the motor side of the MMC.



(b) Motor-side MMC currents in arms and motors.



(c) The motor side current THD is 58.6%.

Fig.31 At 8 Hz, these are the waveforms generated when s/2" equals the torque rating.

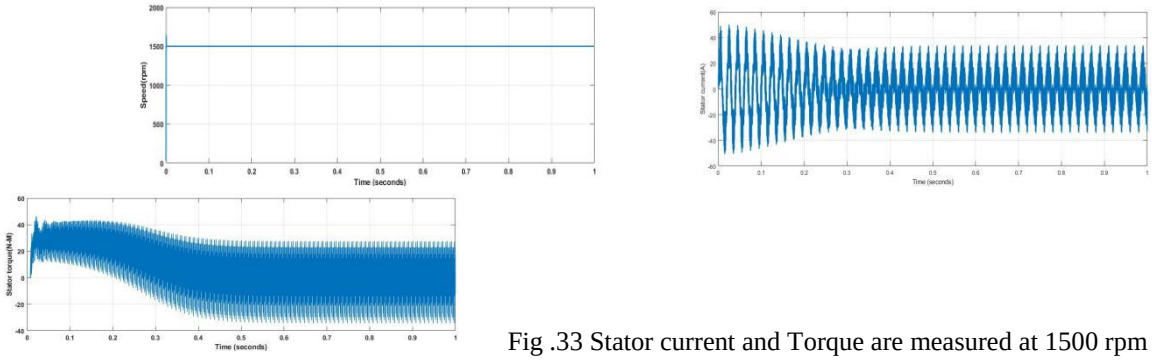


Fig .33 Stator current and Torque are measured at 1500 rpm (existing system)

B) EXTENSION RESULTS (9 LEVEL MMC)

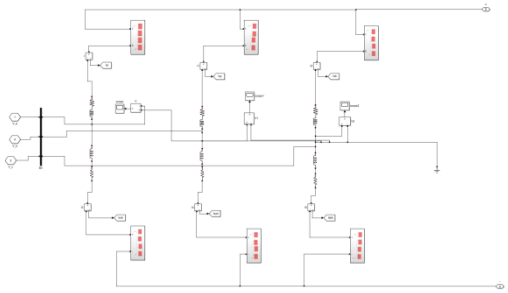


Fig 5.9 a nine-tiered MMC

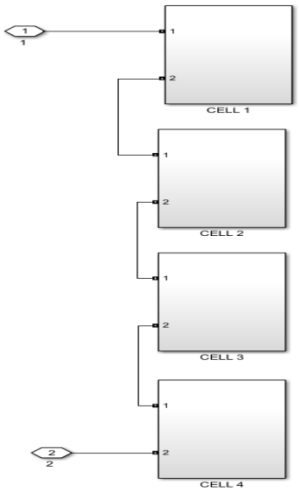


Fig.34 Negative armature of the nine-level subsystem

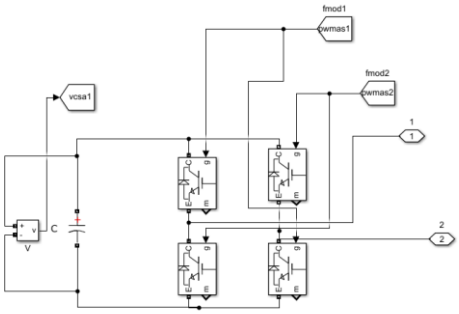


Fig.35 part of the cellular system

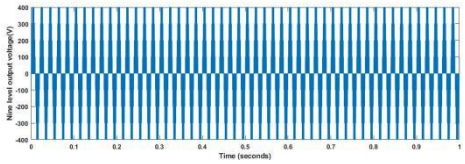


Fig.36 Output voltage has a nine-step range.

CASE-1

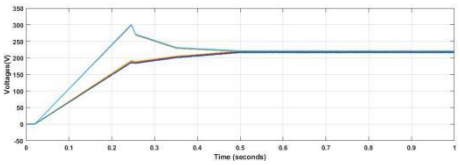


Fig.37 No load on the motor: no balancing control; grid-side MMC SM capacitor voltages.

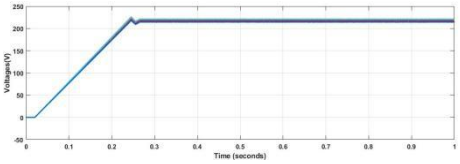


Fig.38 With balancing control and no load on the motor. voltages on the grid-side MMC SM capacitors.

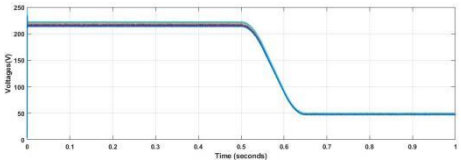


Fig.39 Without balancing control, the voltages of the SM capacitors on the grid-side MMC rise when a rapid motor load is applied.

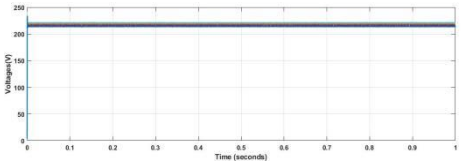


Fig.40 When a sudden increase in motor load is applied, the balancing control is engaged. voltages on the grid-side MMC SM capacitors.

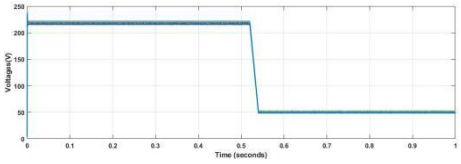


Fig.41 Balancing controls are deactivated if there is a high motor load. Capacitor voltages of one leg

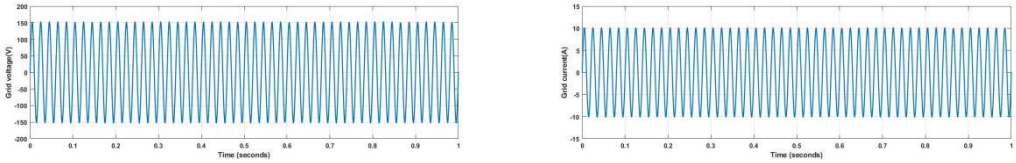


Fig.42 Balancing control can be removed and then re-enabled after a certain amount of time: Voltage and current on the grid

CASE-2

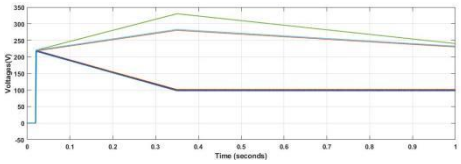


Fig.43 When there is no motor load, balancing control is not necessary Voltages across the SM capacitor on the motor side of the MMC.

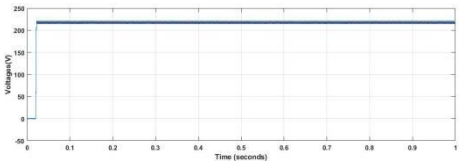


Fig.44 Balancing control with no motor load; SM capacitor voltages on the MMC side.

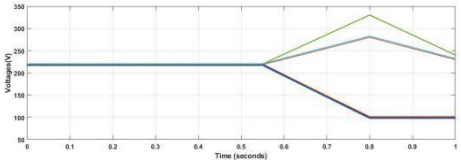


Fig.45 Voltages on the motor side MMC SM capacitor while balancing control is disabled.

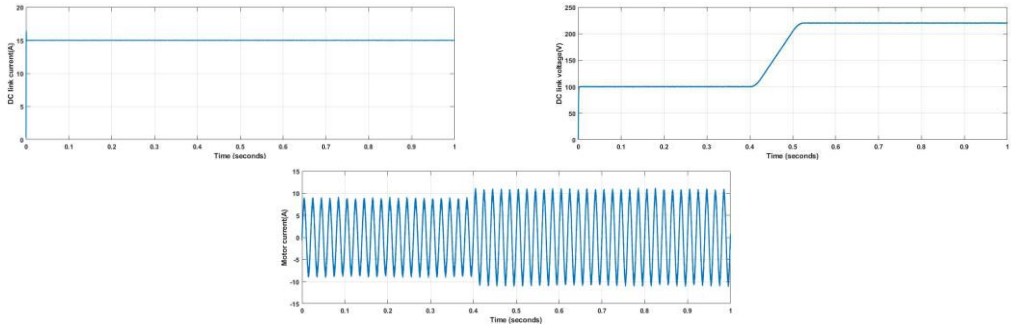
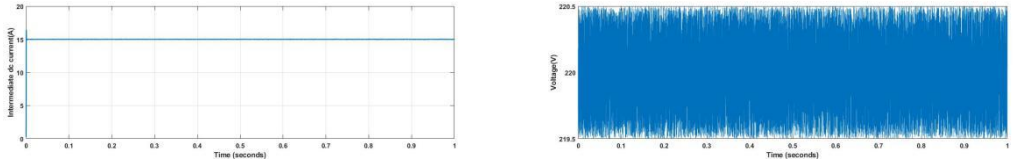
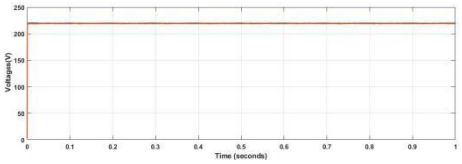


Fig.46 After a period of time, balancing control is disabled and then reactivated. (a) DC-link current, (b) DC-link voltage command, (c) motor current when a sudden motor load is applied.

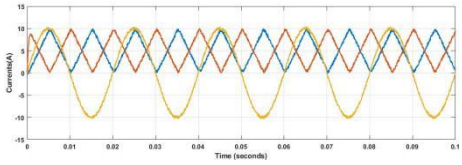
CASE-3



(a)

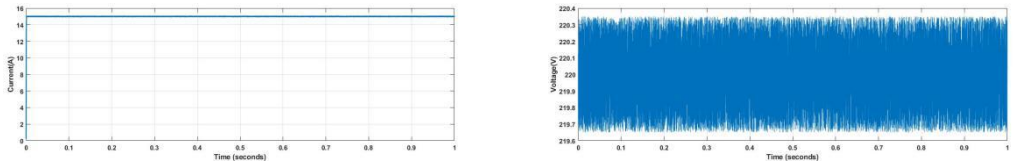


(b)

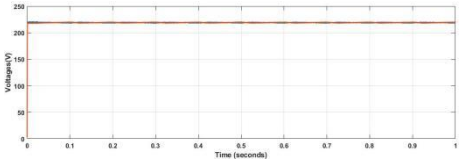


(c)

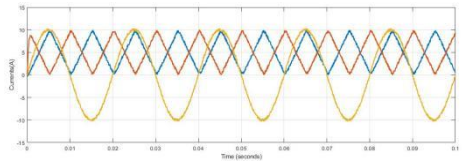
Fig.47 When s/2 = 51 Hz and rated torque is used, the simulated waveforms are shown. (a) Current and voltage in the intermediate dc range. (b) MMC voltages across the SM capacitors on the motor side. (c) MMC arm and motor currents, respectively.



(a)

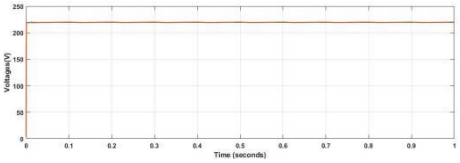


(b)

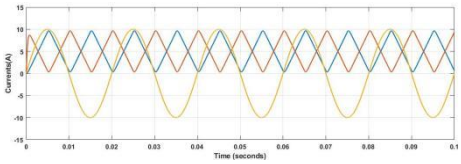


(c)

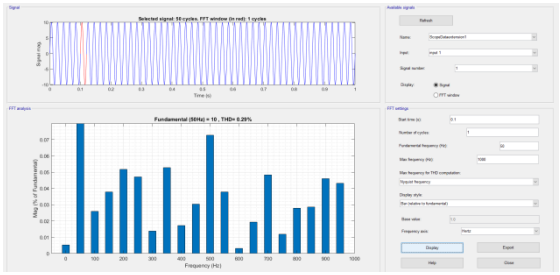
Fig.48 Simulation waveforms for s/2 = 27 Hz and rated torque are shown below. (a) Current and voltage in the intermediate dc range. (b) MMC voltages across the SM capacitors on the motor side. (c) MMC arm and motor currents, respectively.



(a)

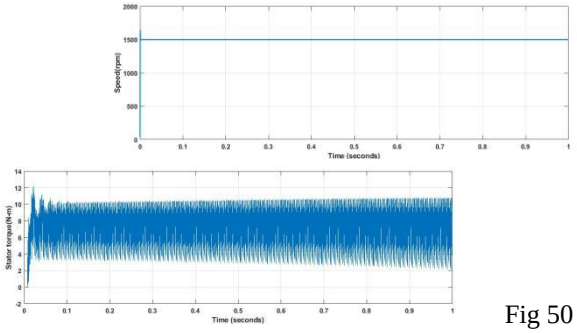


(b)



(c)

Fig.49 At 8 Hz, these are the waveforms generated when s/2" equals the torque rating. voltages of the motor-side MMC's SM capacitor. This includes (b) the arm and motor currents of MMCs on the motor-side. (c)THD of motor current 0.29 %



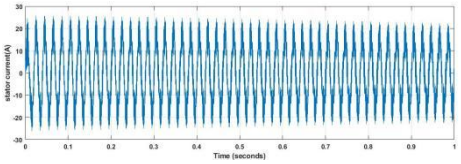


Fig 50 Stator current and Torque are all measured at 1500 rpm (extension system)

THD COMPARISION

	EXISTING SYSTEM	**EXTENSION SYSTEM**
Motor side current THD%	0.58%	0.29%

CONCLUSION

Back-to-back 9-level MMC SM capacitors can be balanced using a fractional order controller explained in this article. This article proposes a voltage-balancing controller for each individual capacitor of the grid and motor side 9level MMCs, but it does not interfere with the average controllers. It has been shown analytically and empirically that the balancing controller works as described. There is no change to the leg-to-leg voltage command in the proposed method. Motor-side MMC capacitors' average voltage V av Cs controller is unaffected by this. Because all SMs have the same capacitance voltage, this technique isn't ideal. These grid-side MMC and motor-side MMC balancing solutions have been empirically proven under various operating situations. The

proposed balance controllers are used to test the drive's overall performance at various speeds. Finally, the simulation comparison between the existing algorithm and the suggested FOPID has been shown.

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